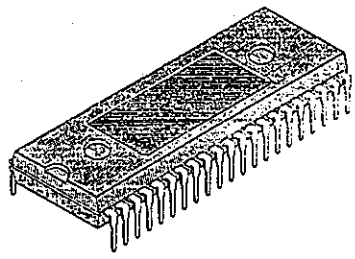
SONY CXA1464AS/CXA1465AS

Color TV Y/C/Jungle/RGB Interface/Deflection Compensation

Description

CXA1464AS/CXA1465AS is bipolar ICs,each having the NTSC color TV luminance signal processing, chrominance signal processing, sync signal processing, RGB interface, auto cut-off, and deflection compensation functions integrated into a chip.

48pin SDIP (Plastic)



Features

- Compatible with I²C bus. Two bus lines SDA and SCL drive 23 self-contained D/A converters to provide various types of adjustments and user controls.
- Has a Deflection compensation circuit which facilitates adjustments for compensation of deflection distortion.
- Has an auto cut-off function for automatic CRT cut-off adjustment and compensation for changes with time.
- Has built-in dynamic picture capability.
- Has multiple inputs (Y/C separate inputs, analog R, G and B inputs, digital R, G and B inputs for screen display).
- Wide band R, G and B interface (typ. −3dB at 20MHz)

Applications

TV sets

Note that the CXA1464AS and CXA1465AS are different in demodulation axis.

CXA1464AS: Compatible with Japanese standard

CXA1465AS: Compatible with U.S.A. standard

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings (Ta=25°C)

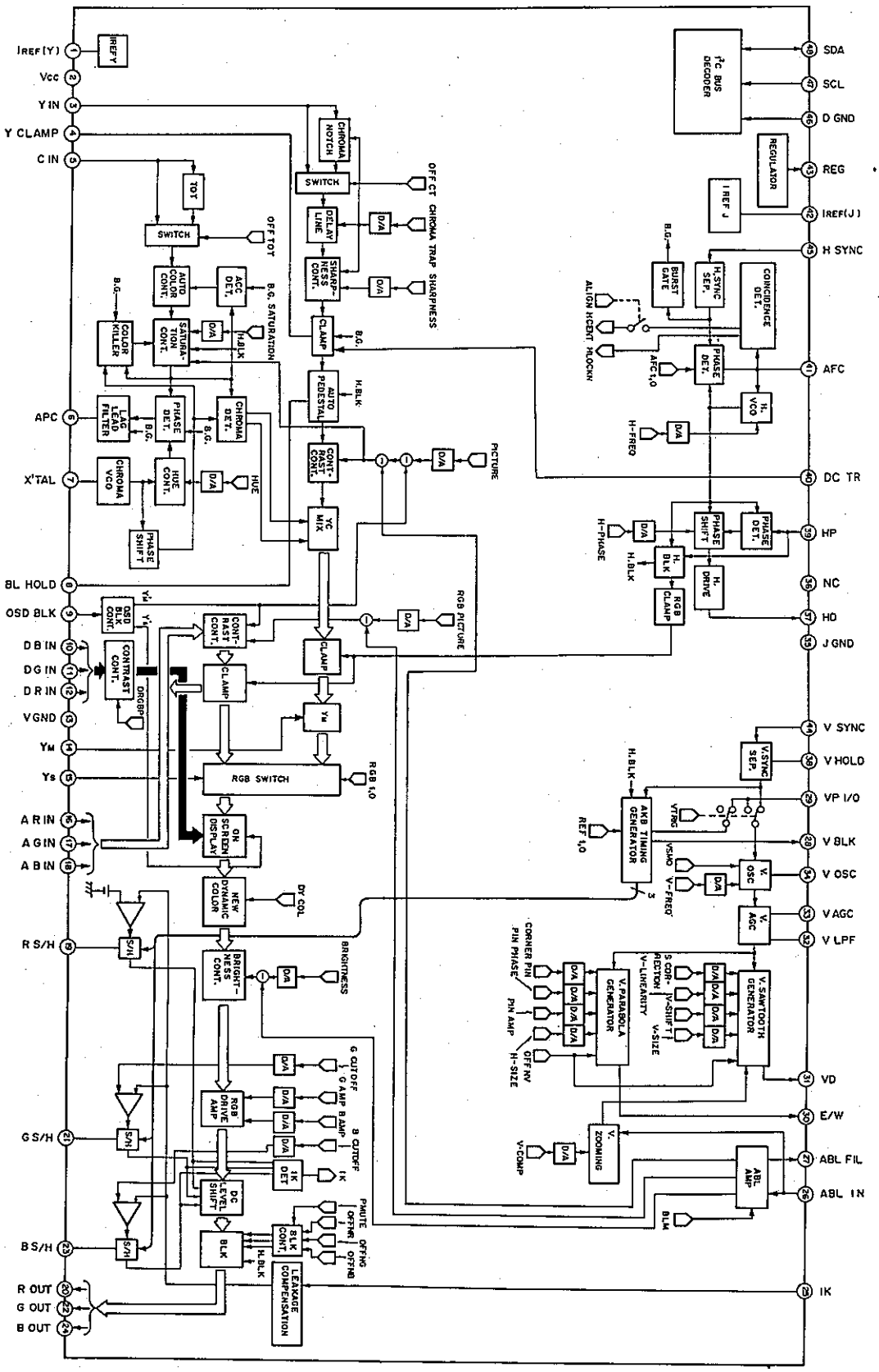
• Supply voltage	V_{CC}	12	V
• Operating temperature	T_{opr}	−20 to +75	°C
• Storage temperature	T_{stg}	−65 to +150	°C
• Allowable power dissipation	P_D	1.9	W

Operating Condition

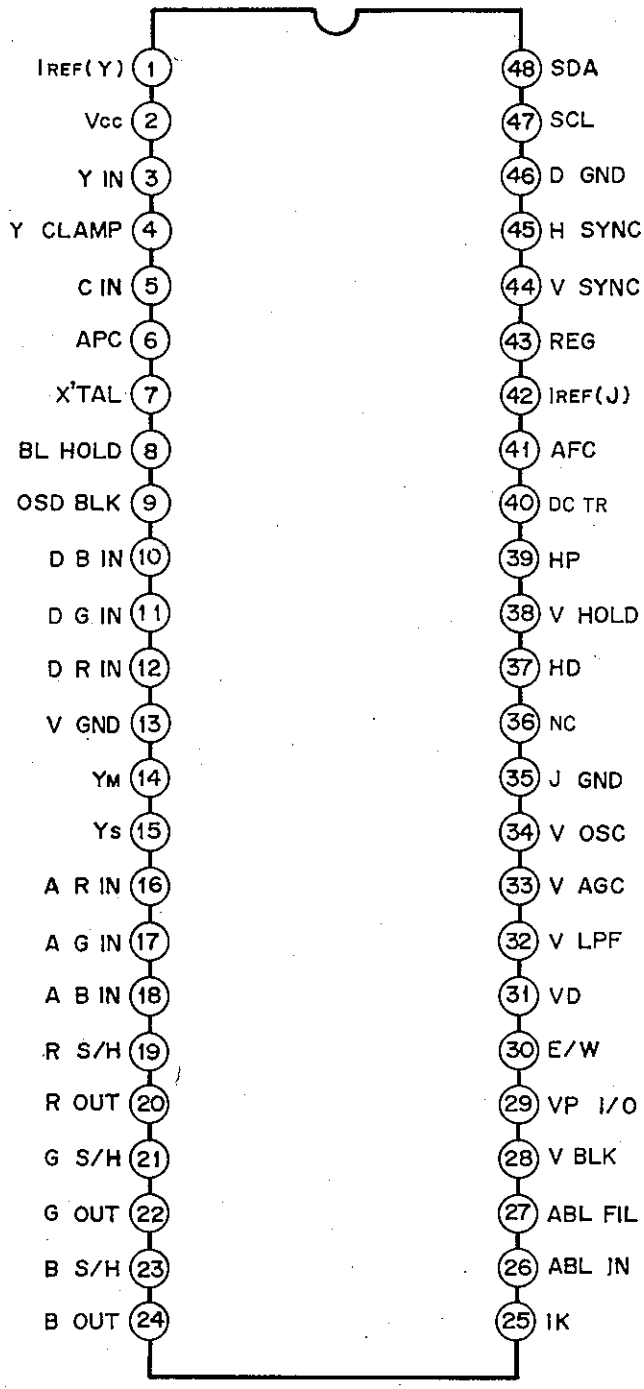
• Supply voltage	V_{CC}	8.5 to 9.5	V

E92202A7X

Block Diagram

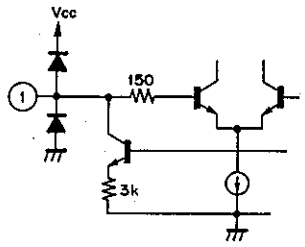
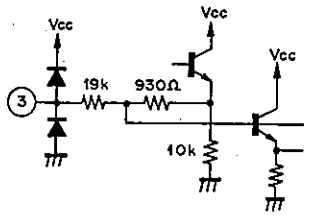
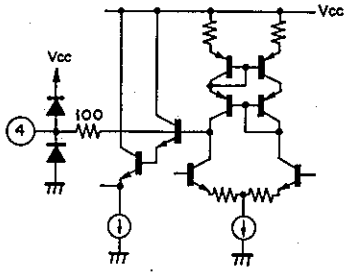
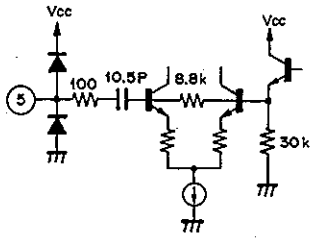
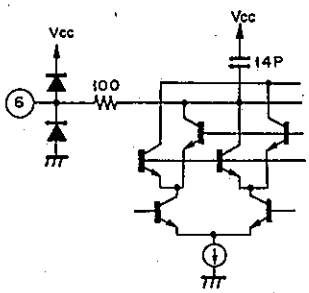
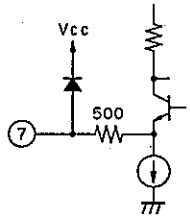


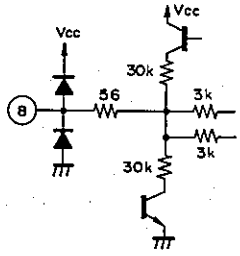
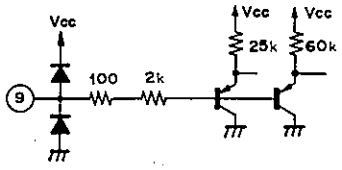
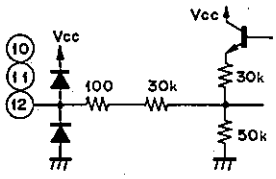
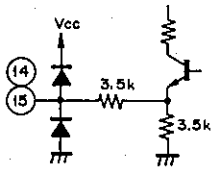
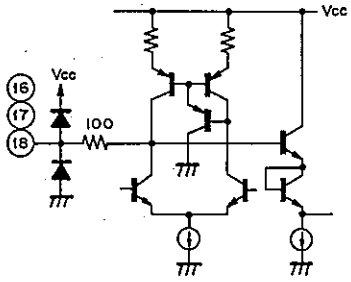
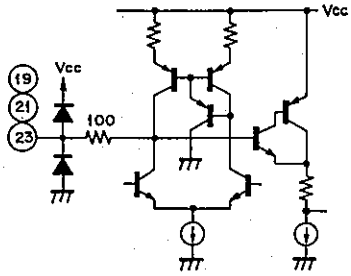
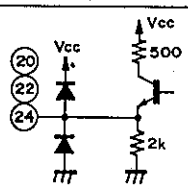
Pin Configuration

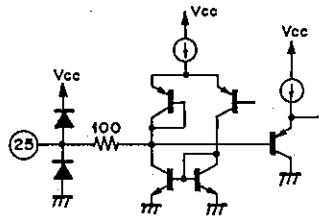
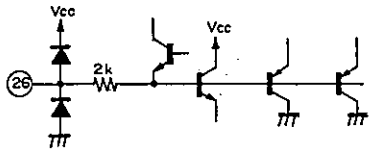
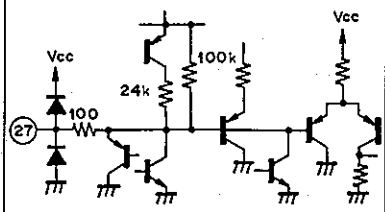
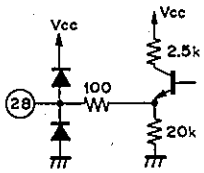
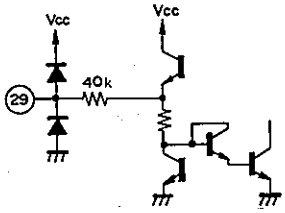
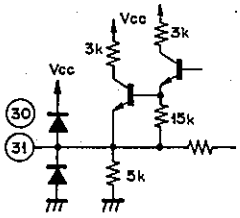
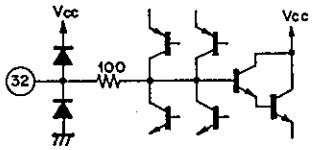
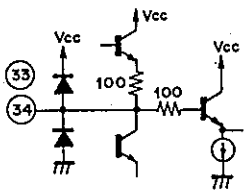


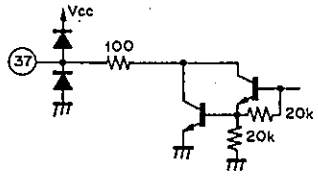
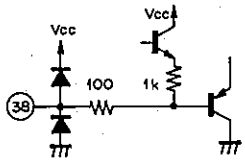
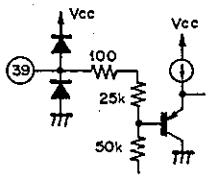
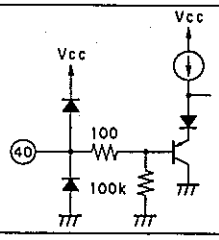
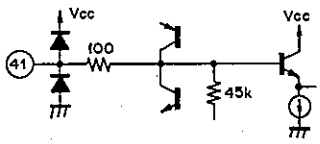
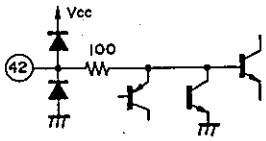
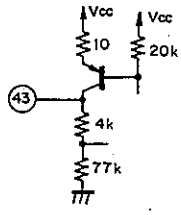
Pin Description

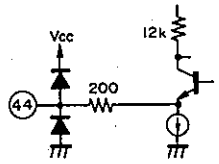
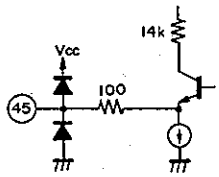
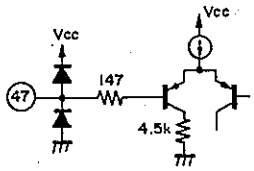
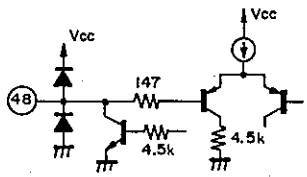
(Pin voltage V_{CC}=9V)

Pin No.	Symbol	Pin Voltage	Equivalent Circuit	Description
1	I_{REF}(Y)	6.4V		Connected to Pin 43 with a resistor in between to produce Y system reference current
2	V_{CC}	9V		Power supply pin
3	Y IN	5V		Y signal input pin. The specified level is 2Vp-p. To be input via a capacitor.
4	Y CLAMP	6V		Y clamp capacitor pin
5	C IN	—		C signal input pin. Specified input levels (chroma burst) Internal TOT OFF 200mVp-p Internal TOT ON 500mVp-p
6	APC	5V		APC lag-lead filter CR connection pin
7	X'TAL	2.6V		Used with a 3.58MHz X'tal connected

Pin No.	Symbol	Pin Voltage	Equivalent Circuit	Description
8	BL HOLD	4V		Pin for connection of capacitor for holding black peak level of dynamic picture (auto pedestal).
9	OSD BLK	—		OSD BLK signal input pin for digital R, G and B inputs
10 11 12	DB IN DG IN DR IN	—		Digital R, G and B input pins for screen display
13	V GND	—		Video system (Y/C/RGB) GND pin
14 15	Y_M Y_S	—		Y_M/Y_S input pins for analog R, G and B inputs V_{IL} max.=0.4V V_{IH} min.=1.0V
16 17 18	AR IN AG IN AB IN	5V		Analog R, G and B input pins. To be input via a capacitor. Specified input level 0.7Vp-p (without sync)
19 21 23	R S/H G S/H B S/H	—		Sample hold pins to connect capacitors to GND for auto cut-off of R, G and B
20 22 24	R OUT G OUT B OUT	—		R, G and B output pins

Pin No.	Symbol	Pin Voltage	Equivalent Circuit	Description
25	I_K	—		Signal which is beam current (I_K) of CRT converted into voltage is to be input via capacitor.
26	ABL IN	—		ABL voltage input pin
27	ABL FIL	—		Connect capacitor for forming LPF for ABL voltage input signal.
28	V BLK	—		V blanking pulse output pin
29	VP I/O	—		V pulse input and output pin
30 31	E/W VD	— —		E/W=Parabolic wave output pin V/D=V drive output pin
32	V LPF	4.2V		Connect capacitor for forming LPF for AGC voltage of V
33 34	V AGC V OSC	—		VAGC is integrating capacitor pin for producing AGCed saw-tooth wave of V. VOSC is integrating capacitor pin for producing saw-tooth wave of V

Pin No.	Symbol	Pin Voltage	Equivalent Circuit	Description
35	J GND	—		GND pin for jungle system (H/V/picture distortion correction)
36	NC	—		No Function
37	HD	—		H drive output pin. This pin is output at open collector.
38	V HOLD	1V		Peak hold pin for sync separation of V. Capacitor to be connected.
39	HP	3V (when there is no signal)		H pulse input pin.
40	DC TR	—		Varies the DC transmission rate. It can be varied between 84 and 100% by changing the voltage applied to pin 40.
41	AFC	2.9V		AFC lag-lead filter CR connection pin.
42	I_{REF}(J)	3.8V		Connected to Pin 43 with a resistor in between to produce jungle system reference current.
43	REG	7.7V		Regulator pin for voltage internally produced from V_{CC} in IC. Capacitor is connected for stabilization.

Pin No.	Symbol	Pin Voltage	Equivalent Circuit	Description
44	V SYNC	1.4V (when there is no signal)		V sync separation input pin. Video signal is input at 2Vp-p.
45	H SYNC	1.4V (when there is no signal)		H sync separation input pin. Video signal is input at 2Vp-p.
46	D GND	—		Digital system GND pin
47	SCL	—		I²C bus standard SCL (Serial CLock) input pin. V_{IL} max.=1.5V V_{IH} min.=3.0V
48	SDA	—		I²C bus standard SDA (Serial DAta) input and output pin. V_{IL} max.=1.5V V_{IH} min.=3.0V V_{OL} max.=0.4V

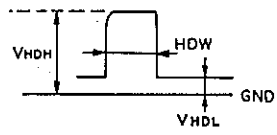
Electrical Characteristics

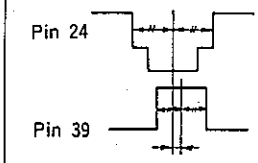
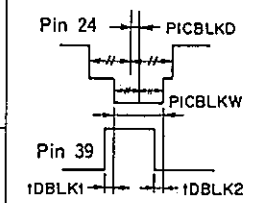
Setting conditions

- Ta=25°C V_{CC}=9V
- I²C bus register should be set at "Test Method, I²C Bus Register Initial Setting" before test.

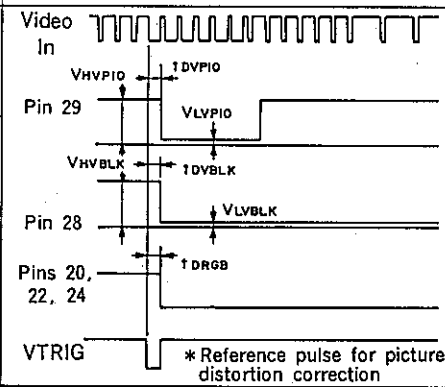
No.	Item	Symbol	Test circuit	Condition	Test pin	Test contents	Min.	Typ.	Max.	Unit
1	Regulator voltage	V_{REG}	I		43	Pin voltage test	7.5	7.75	8.0	V
2	Current consumption	I_{CC}	I		2	Pin inflow current test	65	90	115	mA
3	ABL threshold voltage	V_{ABL}	I		27	Voltage at Pin 26 slowly raised to find voltage that causes voltage at Pin 27 to decrease to less than 6v	0.95	1.05	1.15	V

H system items

4	Horizontal oscillation variable range 1	f_H min 1	2	Pin 40: 0V HFREQ: $7F_H$	37	Frequency test	–	14	15.4	kHz
5	Horizontal oscillation variable range 2	f_H max 1	2	Pin 40: 0V HFREQ: 00H	37	Frequency test	16	17	–	kHz
6	HCENT operation	Δf_{HCENT}	2	Video In: Sig-H1 ALIGN: 1		HFREQ continuously incremented by +1, beginning at 0, until I²C status register HCENT changes from 1 to 0	–	–	–	–
				AFC: 3	37	(Frequency test) −15.734KHz	−50	0	50	Hz
7	Horizontal sync Pull-in range	Δf_{HP-}	2	Video In: Sig-H2, H3		To check that I²C status register HLOCKN is caused to be 1 (pull-in range F_H is shifted from 15.734kHz)	−1.2	−0.9	−0.65	kHz
8		Δf_{HP+}	2	Video In: Sig-H4, H5			0.62	0.9	1.2	kHz
9	AFC gain 1	AFC_{MID}	2	Video In: Sig-H6 AFC: 0	39	Time from fall of Video In to rise at Pin 39: t_-	–	–	–	–
				Video In: Sig-H7 AFC: 0		Time from fall of Video In to rise at Pin 39: t_+, $t_+ - t_-$	0.5	0.6	0.7	μs
10	AFC gain 2	AFC_{LOW}	2	Video In: Sig-H6 AFC: 1	39	Time from fall of Video In to rise at Pin 39: t_-	–	–	–	–
				Video In: Sig-H7 AFC: 1		Time from fall of Video In to rise at Pn 39: t_+, $t_+ - t_-$	0.7	0.85	1.1	μs
11	AFC gain 3	AFC_{HIGH}	2	Video In: Sig-H6 AFC: 2	39	Time from fall of Video In to rise at Pin 39: t_-	–	–	–	–
				Video In: Sig-H7 AFC: 2		Time from fall of Video In to rise at Pin 39: t_+, $t_+ - t_-$	0.25	0.4	0.5	μs
12	HD output pulse width	HDW	2	Video In Sig-H1	37		23	24.5	26	μs
13	HD output high level	V_{HDH}					8.5	9	9.2	V
14	HD output low level	V_{HDL}					0.8	1.05	1.5	V

No.	Item	Symbol	Test circuit	Condition	Test pin	Test contents	Min.	Typ.	Max.	Unit
15	Horizontal phase operating range 1	H_{PHAC}	2	Video In: Sig-Y1 HPHASE: 7	24 39	 Time difference between BOUT center at Pin 24 and HP center at Pin 39 (BOUT)−(HP)	−0.2	0.10	0.3	μs
16	Horizontal phase operating range 2	H_{PHAL}		Video In Sig-Y1 HPHASE: 0			−2.6	−2.2	−1.9	μs
17	Horizontal phase operating range 3	H_{PHAR}		Video In: Sig-Y1 HPHASE: F_H			2.4	2.7	3.0	μs
18	Video horizontal blanking width	P_{ICBLKW}	2	Video In: Sig-Y1	24		9	9.6	10	μs
19	Video horizontal blanking phase	P_{ICBLKD}				Phase difference between video center and blanking center (Video)−(BLK)	−250	0	250	ns
20	HP blanking delay time	t_{DBLK1}			24 39		0	100	200	ns
21	HP blanking delay time	t_{DBLK2}					0	100	200	ns

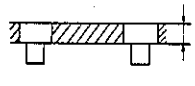
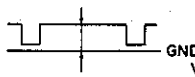
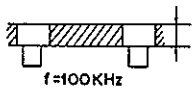
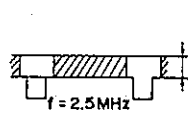
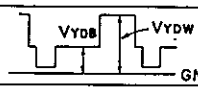
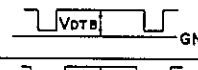
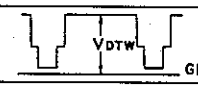
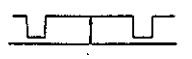
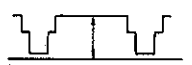
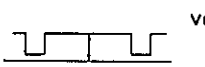
V system items

22	Vertical oscillation variable range 1	f_V min 1	I	VFREQ: $1F_H$	29	Frequency test	–	45	50	Hz
23	Vertical oscillation variable range 2	f_V max 2	I	VFREQ: 0	29	Frequency test	60	65	–	Hz
24	Vertical pull-in range 1	f_{VP1}	I	Video In Sig-V1, 2	29	Frequency pulled when frequency of V of Video In signal is made higher than 55Hz. Synchronized with 63Hz but not with 69Hz.	60	66	70	Hz
25	Vertical oscillation variable range 3	f_V min 2	I	VSMO: 1 VFREQ: $1F_H$		Frequency test	–	37	42	Hz
26	Vertical oscillation variable range 4	f_V max 2	I	VSMO: 1 VFREQ: 0		Frequency test	48	53	–	Hz
27	Vertical pull-in range 2	f_{VP2}	I	VSMO: 1	29	Adjust VFREQ so that frequency at Pin 29 will be 15Hz.	–	–	–	–
				VSMO: 1 Video In: Sig-V3, V4		Frequency pulled when frequency of V of Video In signal is made higher than 45Hz. Synchronized with 73Hz but not with 79Hz.	70	76	80	Hz
28	VP I/O low level	V_{LPIO}	I	Video In: Sig-V5	29	 * Reference pulse for picture distortion correction	0	0.1	0.4	V
29	VP I/O high level	V_{HVPIO}					4.0	5.0	5.5	V
30	VP I/O delay time	t_{HVPIO}					0	20	30	μs
31	V BLK low level	V_{LVBLK}	I	Video In: Sig-V5	28		0	0.1	0.4	V
32	V BLK high level	V_{HVBLK}					4.0	4.6	5.5	V
33	V BLK delay time	t_{DVBLK}					0	20	30	μs
34	RGBD blanking put-off time	t_{DRGB}	I	Video In: Sig-V5	20 22 24		0	20	30	μs

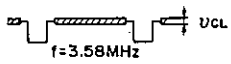
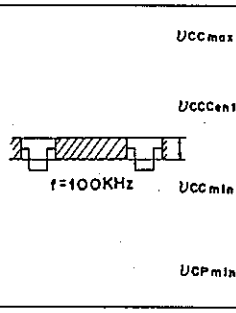
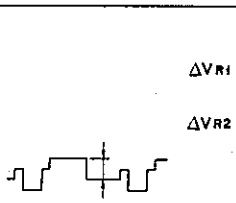
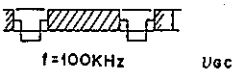
Deflection compensation system items

No.	Item	Symbol	Test circuit	Condition		Test pin	Test contents		Min.	Typ.	Max.	Unit
35	VD output center voltage	$V_{VD,\ CENT}$	I		Video In: Sig-V5	31	Pin 31 waveform (Va, Vb, Vc, 0.1ms, 8.75ms, 16.57ms, GND, VTRIG)	Vb	2.8	2.94	3.1	V
36	V SHIFT variable range 1	ΔV_{SHIFT-}	I	V SHIFT: 0				Vb-$V_{VD,\ CENT}$	−0.13	−0.12	−0.10	V
37	V SHIFT variable range 2	ΔV_{SHIFT+}	I	V SHIFT: $1F_H$				Vb-$V_{VD,\ CENT}$	0.11	0.125	0.14	V
38	V SIZE variable range 1	V_{SIZE}, min	I	V SIZE: 0				Vc-Va	0.8	1.1	1.3	V
39	V SIZE variable 2	$V_{SIZE,}$ max	I	V SIZE: $3F_H$				Vc-Va	1.3	1.6	2.0	V
40	V SCORR variable range 1		I	V SCORR: 0				V_{SS1} a=Va V_{SS1} c=Vc	–	–	–	–
		ΔSa	I	V SCORR: F_H				Va-V_{SS1} a	25	60	88	mV
41	V SCORR variable range 2	ΔSc	I					Vc-V_{SS1} c	−60	−30	−6	mV
42	V LIN variable range 1		I	V LIN: 0				V_{SL1} a=Va V_{SL1} c=Vc	–	–	–	–
		ΔLa	I	V LIN: F_H				Va-V_{SL1} a	80	110	130	mV
43	V LIN variable range 2	ΔL_C	I					Vc-V_{SL1} c	60	90	110	mV
44	EW output center voltage	$V_{EW,CENT}$	I		Video In: sig-V5	30	Pin 30 waveform (Va, Vb, Vc, 0.1ms, 8.75ms, 16.57ms, GND, VTRIG)	Vb	3.9	4.0	4.25	V
45	H SIZE variable range 1	ΔH_{SIZE-}	I	H SIZE: 0				Vb-$V_{EW,CENT}$	−0.61	−0.57	−0.54	V
46	H SIZE variable range 2	ΔH_{SIZE+}	I	H SIZE: $1F_H$				Vb-$V_{EW,CENT}$	0.57	0.61	0.64	V
47	PIN AMP variable range 1	P_{IN} min	I	PIN AMP: 0				Vb-$\frac{Va+Vc}{2}$	0.12	0.18	0.24	V
48	PIN AMP variable range 2	P_{IN} max	I	PIN AMP: $1F_H$				Vb-$\frac{Va+Vc}{2}$	1.0	1.25	1.5	V
49	CORNER PIN variable range	ΔC_{PIN}	I	CORNER PIN: 0				V_{PCP1} a=Va V_{PCP2} a=Vc	–	–	–	–
				CORNER PIN: 7				$\frac{Va+Vc}{2}$ − $\frac{V_{PCP1}a+V_{PCP2}a}{2}$	0.3	0.43	0.6	V
50	PIN PHASE variable range 1		I	PIN PHASE: 0				V_{PHI} a=Va V_{PHI} c=Vc	–	–	–	–
		ΔPPa	I	PIN PHASE: F_H				Va-V_{PHI} a	−0.45	−0.41	−0.35	V
51	PIN PHASE variable range 2	ΔPPc	I					Vc-V_{PHI} c	0.31	0.37	0.41	V
52	V zooming operation 1	ΔV_{SIZE1}	I	Pin 26: 6V V COMP: 0	Video In: Sig-V5	31	Same as No.40 VD center voltage	V_{SIZE1}=Vc-Va	–	–	–	–
			I	Pin 26: 6V V COMP: 7V				V_{SIZE2}=Vc-Va	–	–	–	–
			I	Pin 26: 0V V COMP: 0				V_{SIZE1} (Vc-Va)	0	3	15	mV
53	V zooming operation 2	ΔV_{SIZE2}	I	Pin 26: 0V V COMP: 7				$_{SIZE1}$ (Vc-Va)	35	54	70	mV

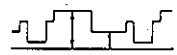
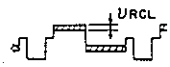
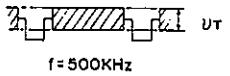
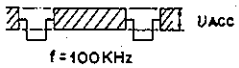
Y system items

No.	Item	Symbol	Test circuit	Condition	Test pin	Test contents		Min.	Typ.	Max.	Unit
54	Chroma trap attenuation	$ATTf_{RAP}$	2	Video In: Sig-Y5 OFFCT: 0 SHARPNESS: F_H	20		$20 \log \frac{\nu_{CT2}}{\nu_{CT1}}$	–	−36	−25	dB
				Video In: Sig-Y5 SHARPNESS: F_H							
55	Y clamp range	ΔV_{YCL}	2	Video In: Sig-HI Pin 3: 6V	20		$V_{YCL2} - V_{YCL1}$	−30	−4	20	mV
				Video In: Sig-HI Pin 3: 4V							
56	R output gain	G_{RW}	2	Video In: Sig-Y2	20		$20 \log \frac{\nu_{RW}}{0.4}$	6	8.5	11	dB
57	G output gain deviation	ΔG_{RG}	2	Video In: Sig-Y2	22		$20 \log \frac{\nu_{GW}}{\nu_{RW}}$	0.5	1.5	2.5	dB
58	B output gain deviation	ΔG_{RB}	2	Video In: Sig-Y2	24		$20 \log \frac{\nu_{BW}}{\nu_{RW}}$	0.5	1.5	2.5	dB
59	Picture variable range	ΔG_{PIX}	2	Video In: Sig-Y2 PICTURE: 0			$20 \log \frac{\nu_{PIX}}{\nu_{RW}}$	–	−26	−18	dB
60	RGB output frequency characteristic 1	Gf_1	2	Video In: Sig-Y3	20 22 24		$20 \log \frac{\nu f_1}{\nu_W}$ $\nu_W = \nu_{RW}, \nu_{GW}, \nu_{BW}$	1	3	5	dB
61	Sharpness control 1	G_S max	2	Video In: Sig-Y3 SHARPNESS: F_H	20		$20 \log \frac{\nu_S MAX}{\nu_{RW}}$	6	7.5	9	dB
62	Sharpness control 2	G_S min	2	Video In: Sig-Y3 SHARPNESS: 0	20		$20 \log \frac{\nu_S min}{\nu_{RW}}$	−7.5	−5.0	−3	dB
63	R output frequency characteristic 2	Gf_2	2	Video In: Sig-Y4	20		$20 \log \frac{\nu f_2}{\nu_{RW}}$	−2.5	0	1.5	dB
64	Y dynamic range	ΔG_{YDR}	2	Video In: Sig-Y6	20		$20 \log \frac{V_{YDW} - V_{YDB}}{1.43} - G_{RW}$	−2	−0.5	1	dB
65	DC transmission rate	G_{DT}	2	Video In: Sig-HI PICTURE: $3F_H$	20		$\frac{V_{DTW} - V_{DTB}}{V_{YDW} - V_{YDB}} \times 100$	80	84	88	%
				Video In: Sig-Y7 PICTURE: $3F_H$	20						
66	Black pull-in amount 1	ΔV_{DP1}	2	Video In: Sig-HI Pin 8: 3V	20		$V_{DP1} - V_{DP2}$	200	300	400	mV
				Video In: Sig-HI Pin 8: 5V							
67	Black pull-in amount 2	ΔV_{DP2}	2	Video In: Sig-Y8 Pin 8: 3V	20		$V_{DP3} - V_{DP4}$	−5	15	35	mV
				Video In: Sig-Y8 Pin 8: 5V							
68	Black pull-in amount 3	ΔV_{DP3}	2	Video In: Sig-HI Pin 8: Voltage source open	20		$V_{DP1} - V_{DP5}$	30	60	90	mV
69	Black pull-in amount 4	ΔV_{DP3}	2	Video In: Sig-Y9 Pin 8: Voltage source open			$V_{DP1} - V_{DP6}$	−170	−120	−70	mV

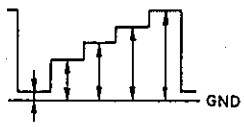
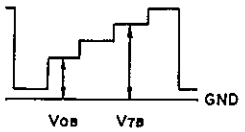
C system items

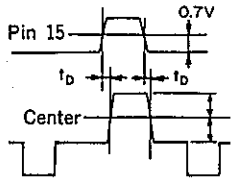
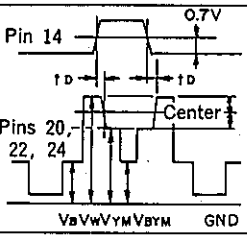
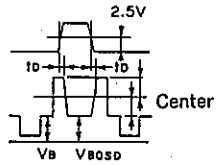
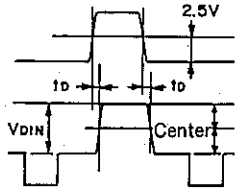
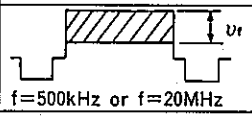
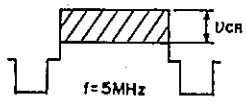
No.	Item	Symbol	Test circuit	Condition	Test pin	Test contents		Min.	Typ.	Max.	Unit
70	APC pull-in range 1	f_{APC1}	2	Video In: Sig-H1 C In: Sig-C1	24		Pull-in at burst frequency ±350Hz	–	–	−350	Hz
71	APC pull-in range 2	f_{APC2}	2	Video In: Sig-H1 C In: Sig-C2	24			350	–	–	Hz
72	Carrier leak	V_{CL}	2	Video In: Sig-H1	24			0	5	50	mVp-p
73	Color output level	V_{CC} max	2	Video In: Sig-H1 C In: Sig-C3	24			0.8	1.1	1.8	Vp-p
74	Color control characteristic 1	G_{CC} cent	2	Video In: Sig-H1 C In: Sig-C3 SATURATION: $3F_H$	24		$20 \log \frac{V_{CC}\ cent}{V_{CC}\ max}$	−6	−4.8	−3.0	dB
75	Color control characteristic 2	G_{CC} min	2	Video In: Sig-H1 C In: Sig-C3 SATURATION: 0	24		$20 \log \frac{V_{CC}\ min}{V_{CC}\ max}$	–	−55	−40	dB
76	Chroma picture variable range	G_{CP}	2	Video In: Sig-H1 C In: Sig-C3 PICTURE: 0	24		$20 \log \frac{V_{CP}\ min}{V_{CC}\ max}$	–	−25	−18	dB
77	Detection axis R	ϕ_R	2	Video In: Sig-H1 C In: Sig-C4 PICTURE: $1F_H$	20		$90° - \tan^{-1} \frac{\Delta V_{R2}}{\Delta V_{R1}}$	※ 91 (107)	98 (114)	105 (121)	deg
				Video In: Sig-H1 C In: Sig-C5 PICTURE: $1F_H$	20						
78	Detection axis R	ϕ_G	2	Video In: Sig-H1 C In: Sig-C4 PICTURE: $1F_H$	22		$270° - \tan^{-1} \frac{\Delta V_{G2}}{\Delta V_{G1}}$	※ 236 (248)	243 (255)	250 (262)	deg
				Video In: Sig-H1 C In: Sig-C5 PICTURE: $1F_H$	22						
79	Detection output ratio R	G_R	2	Video In: Sig-H1 C In: Sig-C3	20		$\frac{V_{RC}}{V_{CC}\ max} \cdot \frac{V_{RW}}{V_{RW}}$	0.67	0.78	0.9	–
80	Detection output ratio G	G_G			22		$\frac{V_{GC}}{V_{CC}\ max} \cdot \frac{V_{BW}}{V_{GW}}$	0.27	0.31	0.36	–

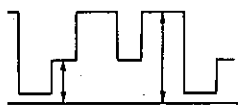
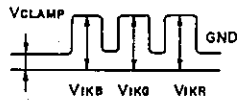
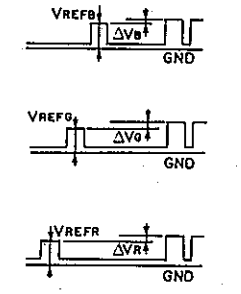
※ The value in brackets is the value of CXA1465AS

No.	Item	Symbol	Test circuit	Condition	Test pin	Test contents		Min.	Typ.	Max.	Unit
81	HUE variable range 1	ϕ_-	2	Video In: Sig-H1 C In: Sig-C4, C5 PICTURE: $1F_H$, HUE: 0	24	 CIn: Sig-C4 V_{C1} V_{C2} CIn: Sig-C5 V_{C3} V_{C4}	$\tan^{-1}\frac{V_{C1-}V_{C2}}{V_{C4-}V_{C3}}$	–	−38	−28	deg
82	HUE variable range 2	ϕ_C	2	Video In: Sig-H1 C In: Sig-C4, C5 PICTURE: $1F_H$, HUE: $3F_H$				0	9	18	deg
83	HUE variable range 3	ϕ_+	2	Video In: Sig-H1 C In: Sig-C4, C5 PICTURE: $1F_H$, HUE: $7F_H$				42	48	–	deg
84	Residual carrier level	V_{RCL}	2	Video In: Sig-H1 C In: Sig-C4	24		3.58MHz component +7.16MHz component	0	10	100	mVp-p
85	Chroma frequency characteristic −	G_{T-}	2	Video In: Sig-H1 C In: Sig-C6 (−500KHz)		 f=500KHz	$20\log\frac{\nu_T}{\nu_{CC}\ max}$	−9	−4	0	dB
86	Chroma frequency characteristic +	G_{T+}	2	Video In: Sig-H1 C In: Sig-C7 (+500KHz)				−3.5	−1.5	0.5	dB
87	Chroma frequency characteristic 2	GTOFF	2	Video In: Sig-H1 C In: Sig-C6 OFFTOT: 1				−3.5	−1.5	0.5	dB
88	ACC amplitude characteristic +	G_{ACC+}	2	Video In: Sig-H1 C In: Sig-C8 (+6dB)		 f=100KHz	$20\log\frac{\nu_{ACC}}{\nu_{CC}\ max}$	−0.5	0.2	1.5	dB
89	ACC amplitude characteristic −	G_{ACC-}	2	Video In: Sig-H1 C In: Sig-C9 (−20dB)				−8	−1.2	0	dB
90	Killer point	KP	2	Video In: Sig-H1 C In: Sig-C10, C11			Check that output ceases to appear at −41dB and appears at −24dB.	−41	−30	−24	dB

RGB interface system items

No.	Item	Symbol	Test circuit	Condition		Test pin	Test contents		Min.	Typ.	Max.	Unit
91	A-IN gain 1	G_{AIN}	2	RGBPIX: $7F_H$	Video In: Sig-H1 AIn: Sig-R1 Pin 15: 1.4V	20 22 24		$20\log\frac{V_{7A-}V_{0A}}{0.7}$	9	10	11	dB
92	A-IN linearity	L_{EXT}	2					$\frac{V_{10A-}V_{0A}}{2(V_{5A-}V_{0A})}\times100$	95	98	100	%
93	A-IN gain deviation	ΔG_{AIN}	2						1.1	1.7	2.3	dB
94	Blanking level	V_{BLK}	2					V_{BLK}	0	0.25	0.4	V
95	A-IN gain 2	G_{PIX}	2	RGBPIX: 0		20 22 24		$20\log\frac{V_{7B-}V_{0B}}{0.7}$	−14.5	−13.5	−12	dB
96	Drive variable range	G_{DRIVE}	2	GAMP: 0 BAMP: 0		22 24		$20\log\frac{V_{7B-}V_{0B}}{V_{7A-}V_{0A}}$	−6.5	−5.5	−4.5	dB
97	Dynamic color operation R	D_{COLR}	2	DYCOL: 1		20		$\frac{V_{7B-}V_{0B}}{V_{7A-}V_{0A}}\times100$	94.5	97	98.5	%
98	Dynamic color operation G	D_{COLG}	2			22			98	100	102	%
99	Dynamic color operation B	D_{COLB}	2			24			104	106	108	%
100	Dynamic color offset	ΔV_{DCOL}	2			20 22 24		$V_{0B-}V_{0A}$	−30	0	30	mV

No.	Item	Symbol	Test circuit	Condition	Test pin	Test contents		Min.	Typ.	Max.	Unit
101	Ys delay time	t_{DYS}	2	Video In: Sig-H1 A In: Sig-R2 Pin 15: SIG-R3	20 22 24		t_D	0	50	70	ns
102	Y_M delay time	t_{DYS}	2	Video In: Sig-Y10 Pin 15: SIG-R3	20 22 24		t_D	0	30	70	ns
103	Y_M attenuation	G_{YM}					20 log $\frac{V_{YM-}V_B}{V_{W-}V_B}$	−6.4	−5.4	−4.4	dB
104	Y_M Black variation	ΔV_{YM}					$V_{B-}V_{BYM}$	−30	25	120	mV
105	OSDBLK delay time	t_{DOSD}	2	Video In: Sig-HI A In: Sig-R5 Pin 9: Sig-R7	20 22 24		t_D	0	40	70	ns
106	OSDBLK black variation	ΔV_{OSD}					$V_{B-}V_{BOSD}$	−150	130	400	mV
107	DIN delay time	t_{DDIN}	2	Video In: Sig-HI D In: Sig-R6	20 22 24		t_D	0	30	70	ns
108	DIN level H	V_{DH}	2	DRGBP: 0	20		V_{DIN}	1.55	1.8	2.05	V
					22 24			1.95	2.2	2.45	
109	DIN level L	V_{DL}	2	DRGBP: 1	20		V_{DIN}	1.25	1.45	1.65	V
					22 24			1.5	1.75	2.0	
110	AIN frequency characteristic	G_{FREQ}	2	Video In: Sig-HI A In: Sig-R7, R8 (R7: 500KHz, R8: 20MHz)	20 22 24		20 log $\frac{\nu f\ (20M)}{\nu f\ (500K)}$	−5	−3	0	dB
111	Crosstalk 1	G_{CROS1}	2	Video In: Sig-Y14 Pin 15: 0V/1.4V	20 22 24		20 log $\frac{\nu_{CR}(1.4V)}{\nu_{CR}(0V)}$	–	−60	−50	dB
112	Crosstalk 2	G_{CROS1}	2	Video In: Sig-HI A In: Sig-R9 Pin 15: 0V/1.4V			20 log $\frac{\nu_{CR}(0V)}{\nu_{CR}(1.4V)}$	–	−60	−50	dB

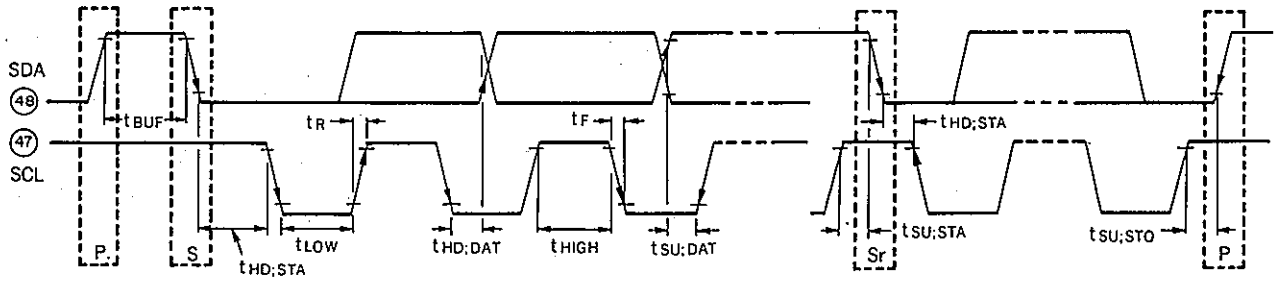
No.	Item	Symbol	Test circuit	Condition		Test pin	Test contents		Min.	Typ.	Max.	Unit
113	ABL operation 1	G_{ABL11}	2	BRIGHTNESS: $7F_H$ BLM: 1	Video In: Sig-Y10 Pin 27: 8V/5V/2V	20	 GND Pin 27 8V V_{BA1} V_{WA1} Pin 27 5V V_{BA2} V_{WA2} Pin 27 2V V_{BA3} V_{WA3}	$20 \log \frac{V_{WA2-}V_{BA2}}{V_{WA1-}V_{BA1}}$	–	−10	−6	dB
114	ABL operation 2	V_{ABL11}						$V_{BA2-}V_{BA1}$	−50	0	50	mV
115	ABL operation 3	G_{ABL12}						$20 \log \frac{V_{WA3-}V_{BA3}}{V_{WA1-}V_{BA1}}$	–	−42	−19	dB
116	ABL operation 4	V_{ABL12}						$V_{BA3-}V_{BA1}$	–	−1.4	−1.0	V
117	ABL operation 5	G_{ABL2}	2	BRIGHTNESS: $7F_H$ BLM: 0	Video In: Sig-Y10 Pin 27: 8V/5V	20		$20 \log \frac{V_{WA2-}V_{BA2}}{V_{WA1-}V_{BA1}}$	–	−3	−1.5	dB
118	ABL operation 6	V_{ABL2}						$V_{BA2-}V_{BA1}$	–	−0.5	−0.4	V
119	A-IN ABL operation 1	G_{ABL31}	2	BRIGHTNESS: $7F_H$ BLM: 1	Video In: Sig-H1 A In: Sig-R1 Pin 27: 8V/5V/2V	20	 GND Pin 27 8V V ϕ_{A1} V_{7A1} Pin 27 5V V ϕ_{A2} V_{7A2} Pin 27 2V V ϕ_{A3} V_{7A3}	$20 \log \frac{V_{7A2-}V_{0A2}}{V_{7A1-}V_{0A1}}$	–	−8	−4.5	dB
120	A-IN ABL operation 2	V_{ABL31}						$V_{0A2-}V_{0A1}$	−50	0	50	mV
121	A-IN G_{ABL32} operation 3	G_{ABL32}						$20 \log \frac{V_{7A3-}V_{0A3}}{V_{7A1-}V_{0A1}}$	–	−18	−8	dB
122	A-IN ABL operation 4	V_{ABL32}						$V_{0A3-}V_{0A1}$	–	−1.4	−1.1	V
123	I_K clamp level	V_{CLAMP}	3		Video In: Sig-V5 Pin 15: 1.4V	25	 VCLAMP GND VIKB VIKG VIKR	V_{CLAMP}	1.25	1.35	1.45	V
124	I_K R level	V_{IKR}						V_{IKR}	2.15	2.25	2.35	V
125	I_K vriable range 1	V_{IK} max	3	GCUT OFF: F_H BCUT OFF: F_H				V_{IKG}, V_{IKB}	2.45	2.55	2.65	V
126	I_K vriable range 2	V_{IK} min	3	GCUT OFF: 0 BCUT OFF: 0					1.55	1.65	1.75	V
127	RGB output DC range 1	V_{REF} max	1	Video in: Sig-V5 Pin 15: 1.4V V_{SH}: 4.6V		20 22 24	 VREFB ΔVB GND VREFG ΔVG GND VREFR ΔVR GND	V_{REFR}, V_{REFG}, V_{REFB}	3.0	3.3	3.7	V
128	RGB output DC range 2	V_{REF} min	1	Video in: Sig-V5 Pin 15: 1.4V V_{SH}: 8V					0.5	0.85	1.3	V
129	BRIGHT variable range 1	V_{BRT} min	1	BRIGHTNESS: 0	Video In: Sig-V5 Pin 15: 1.4V			ΔV_R, ΔV_G, ΔV_R	−1.4	−1.0	−0.8	V
130	BRIGHT variable range 2	V_{BRT} max	1	BRIGHTNESS: $7F_H$					0.24	0.3	0.41	V
131	A-IN DC offset	ΔV_{AIN}	1	BRIGHTNESS: Adjustment	Video In: Sig-V5 Pin 15: 1.4V			First adjust BRIGHTNESS to reduce ΔV_R to a minimum. Offset voltage between Pins 20, 22 and 24 (ΔV_R, ΔV_G, ΔV_R)	−30	0	30	mV
132	Y-IN DC offset	ΔV_{YIN}	1	BRIGHTNESS: Adjustment	Video In: Sig-V5				−30	0	30	mV

I²C Bus Items (SDA, SCL)

No.	Item	Symbol	Min.	Typ.	Max.	Unit
133	High level input voltage	V_{IH}	3.0	—	5.0	V
134	Low level input voltage	V_{IL}	0	—	1.5	V
135	High level input voltage	I_{IH}	—	—	10	μA
136	Low level input voltage	I_{IL}	—	—	10	μA
137	Low level output voltage (during SDA (Pin 48) 3mA inflow)	V_{OL}	0	—	0.4	V
138	Maximum inflow current	I_{OL}	3	—	—	mA
139	Input capacitance	C_I	—	—	10	pF
140	Maximum clock frequency	f_{SCL}	0	—	100	kHz
141	Data change minimum waiting time	t_{BUF}	4.7	—	—	μs
142	Minimum waiting time at start of data transfer	$t_{HD:STA}$	4.0	—	—	μs
143	Low level clock pulse width	t_{LOW}	4.7	—	—	μs
144	High level clock pulse width	t_{HIGH}	4.0	—	—	μs
145	Minimum waiting time for start preparation	$t_{SU:STA}$	4.7	—	—	μs
146	Minimum data hold time	$t_{HD:DAT}$	5	—	—	μs
147	Minimum data preparation time	$t_{SU:DAT}$	250	—	—	ns
148	Rise time	t_R	—	—	1	μs
149	Fall time	t_F	—	—	300	ns
150	Minimum waiting time for stop preparation	$t_{SU:STO}$	4.7	—	—	μs

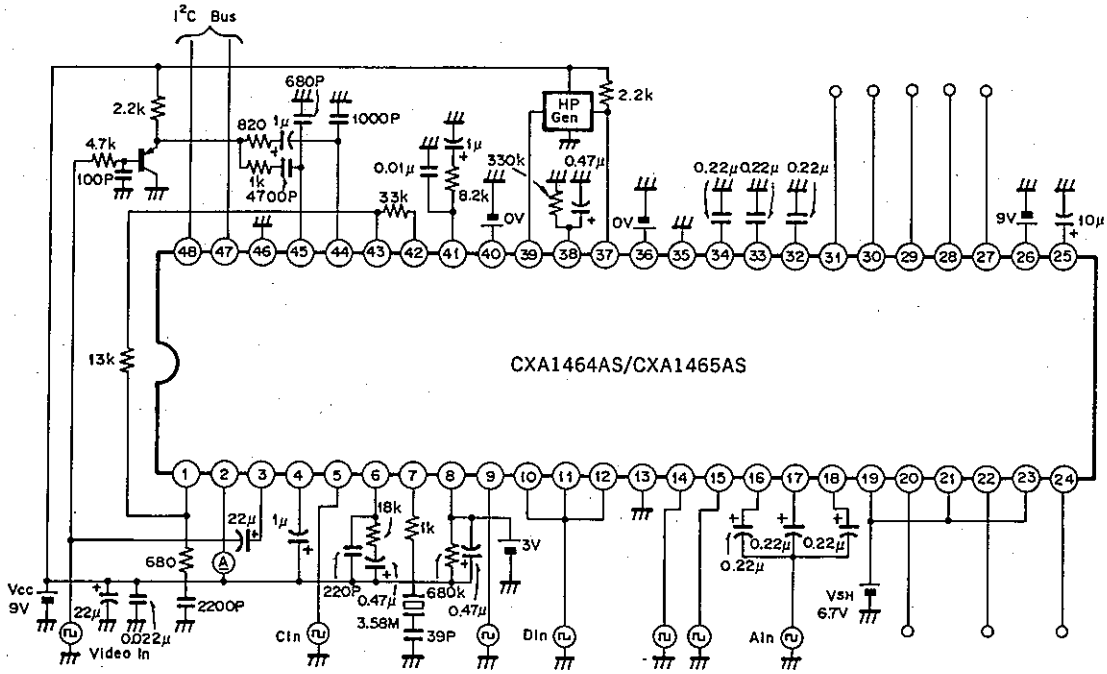
I²C bus load conditions: Pll up resistor 4kΩ (Connect to +5V)
Load capacity 200pF (Connect to GND)

I²C Bus Control Signal



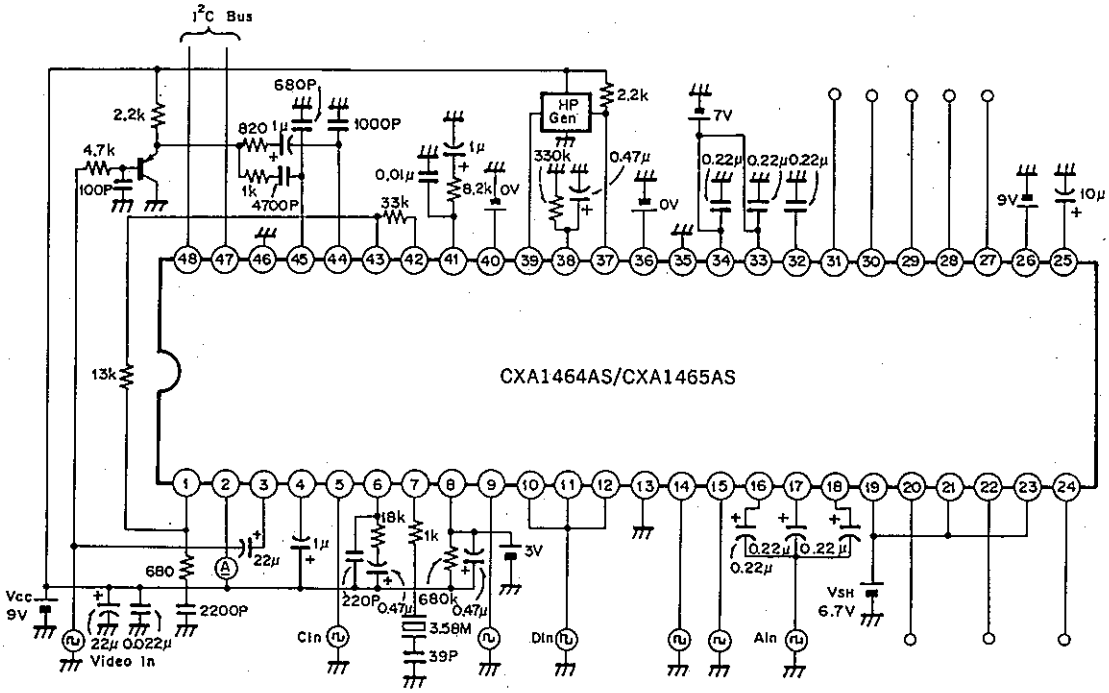
Electrical Characteristics Test Circuit

Test circuit 1



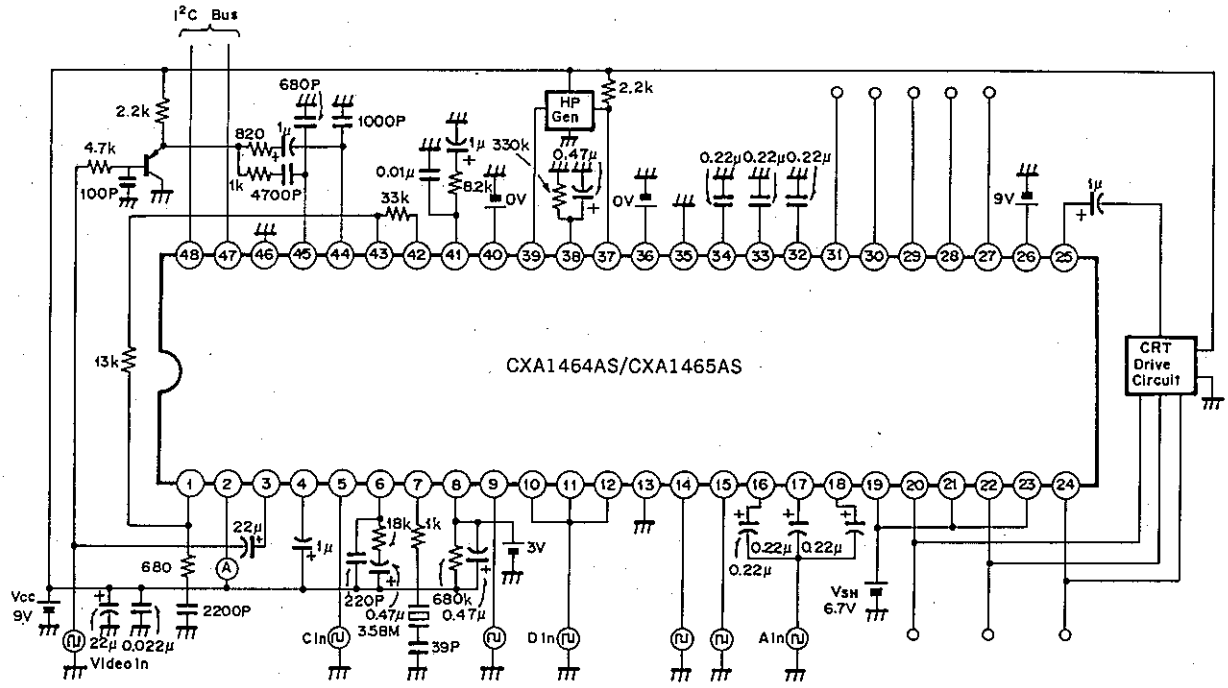
※ All ⓝ except those specified in the "Condition" column of the electrical characteristics should be connected to GND.

Test circuit 2



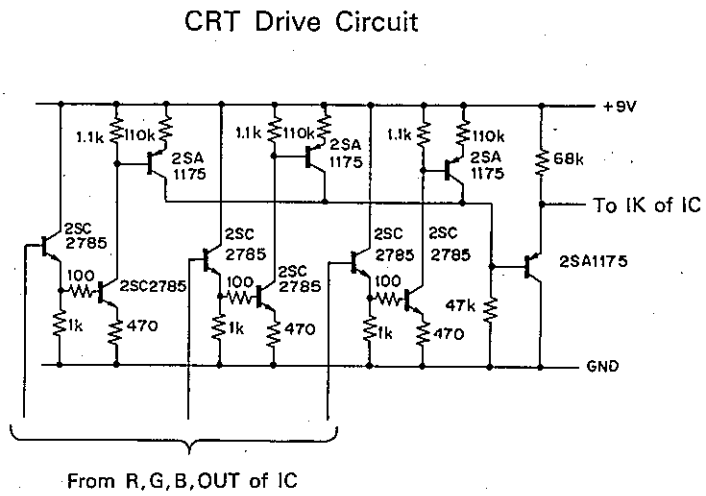
※ All ⓝ except those specified in the "Condition" column of the electrical characteristics should be connected to GND.

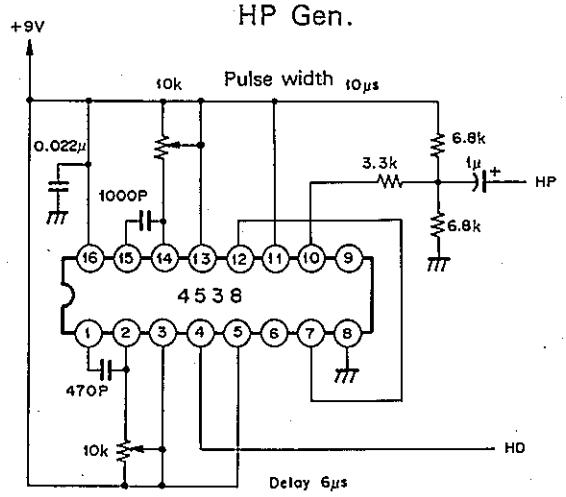
Test circuit 3



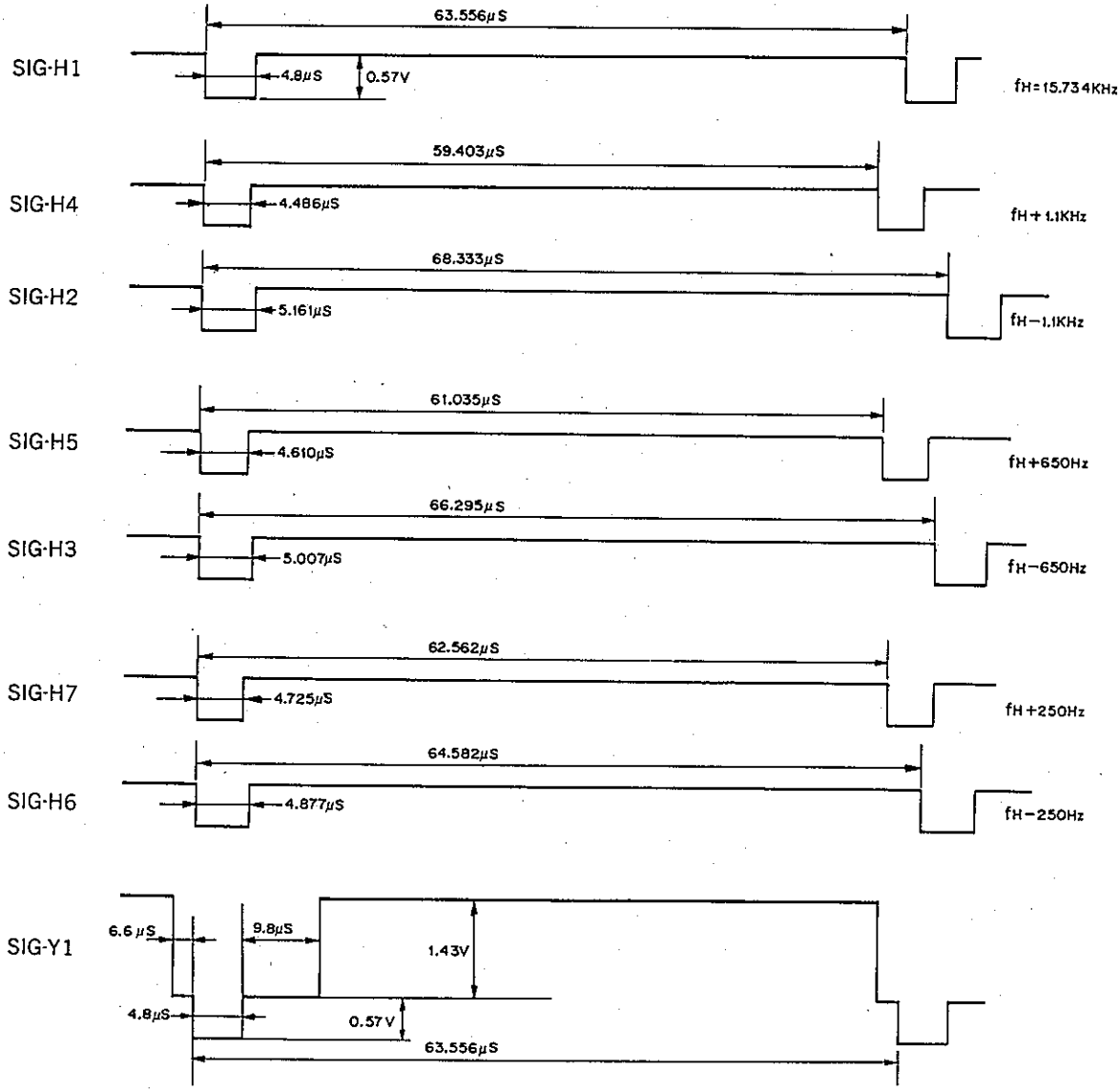
※ All ⓝ except those specified in the "Condition" column of the electrical characteristics should be connected to GND.

Reference Circuit

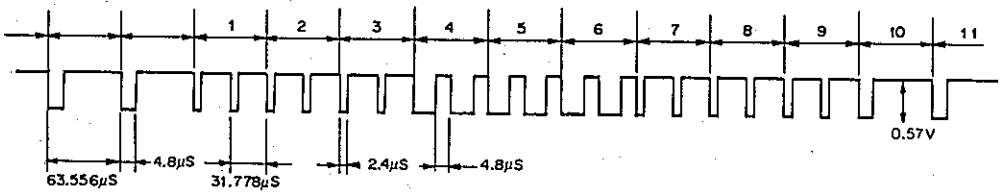




Video Signals Used for Test
H system test signals



V and Deflection compensation systems test signals

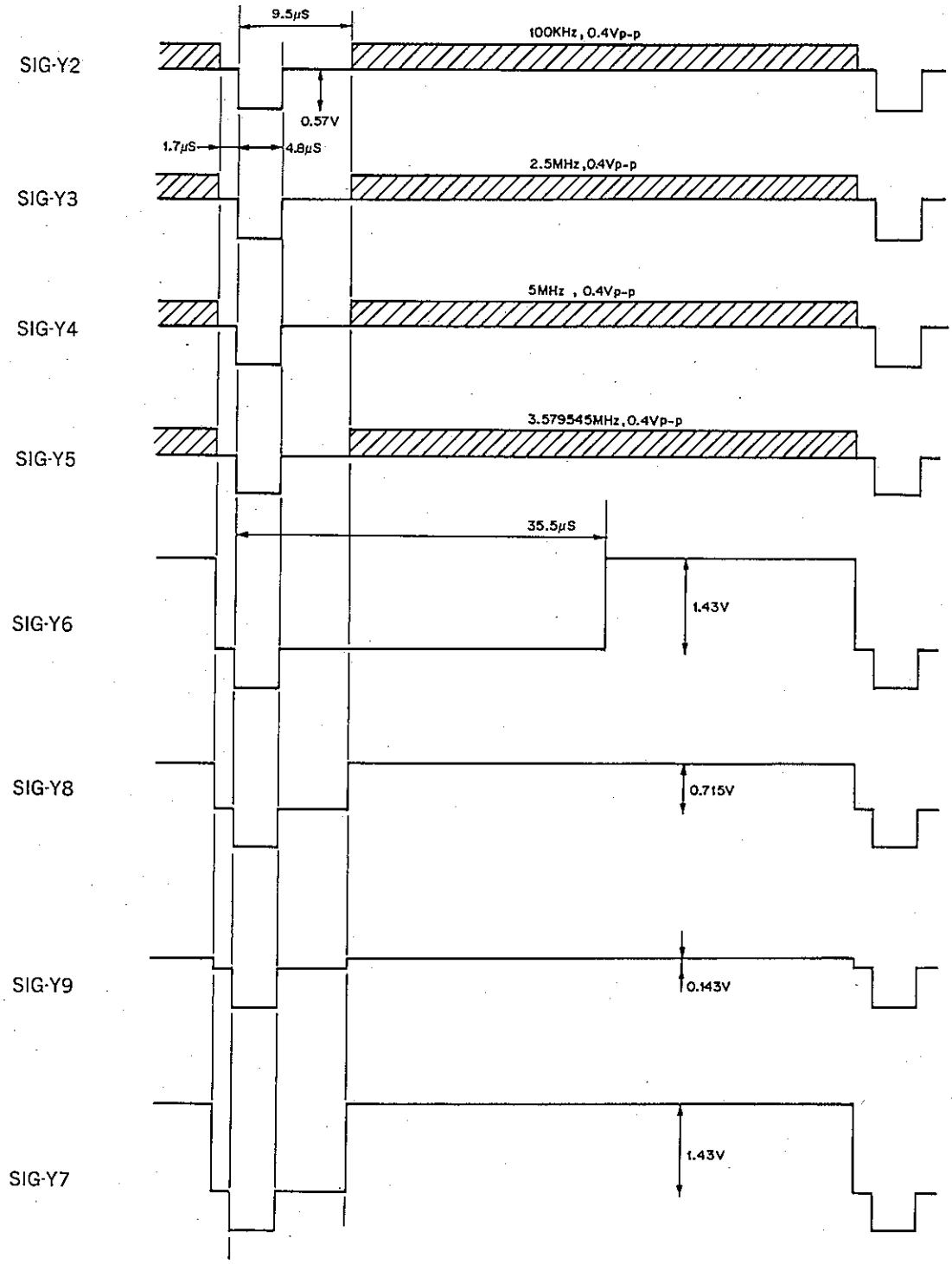


SIG-V1 $f_V = f_H/250$ SIG-V4 $f_V = f_H/199$

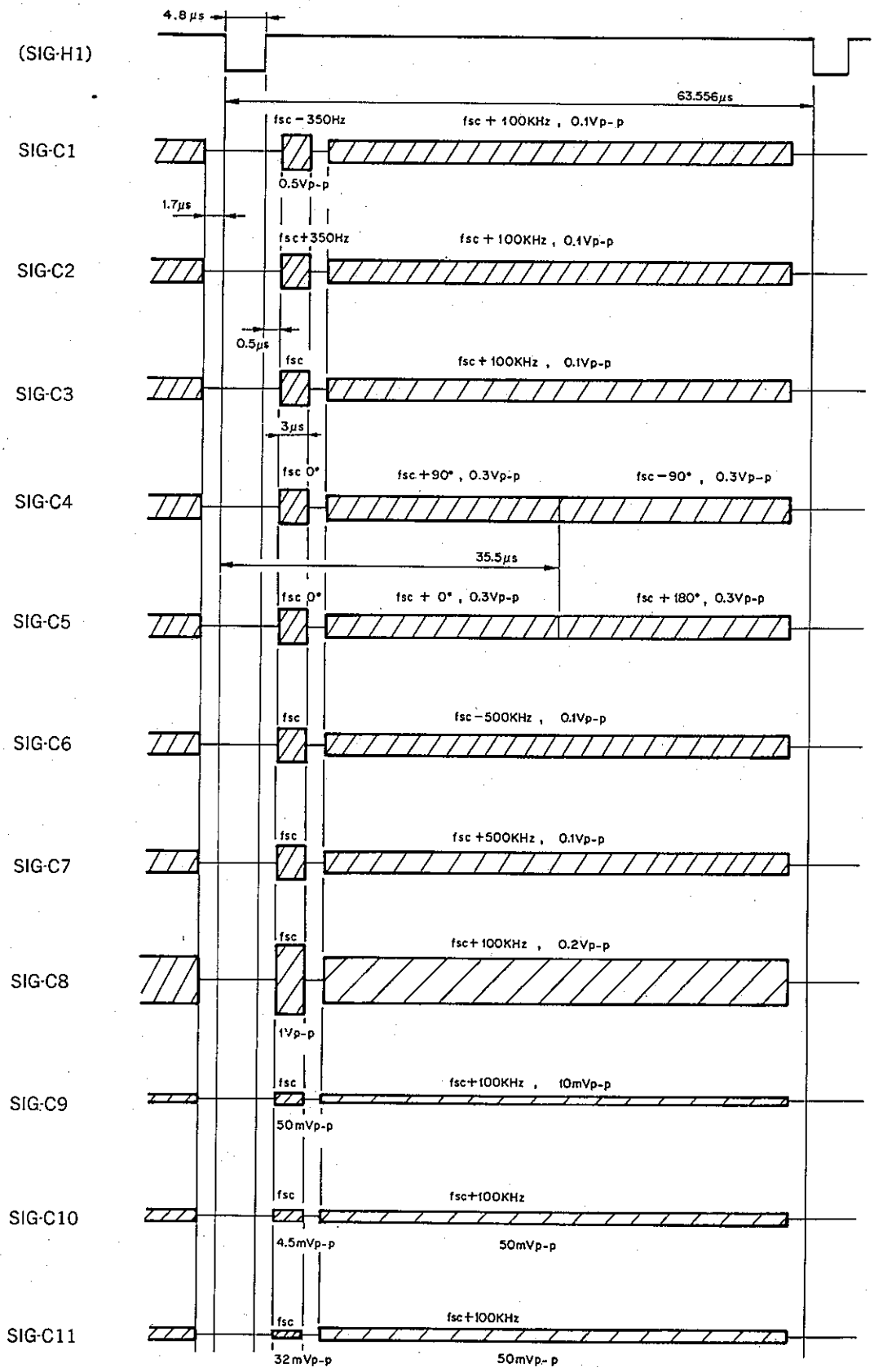
SIG-V2 $f_V = f_H/228$ SIG-V5 $f_V = f_H/262$

SIG-V3 $f_V = f_H/215.5$

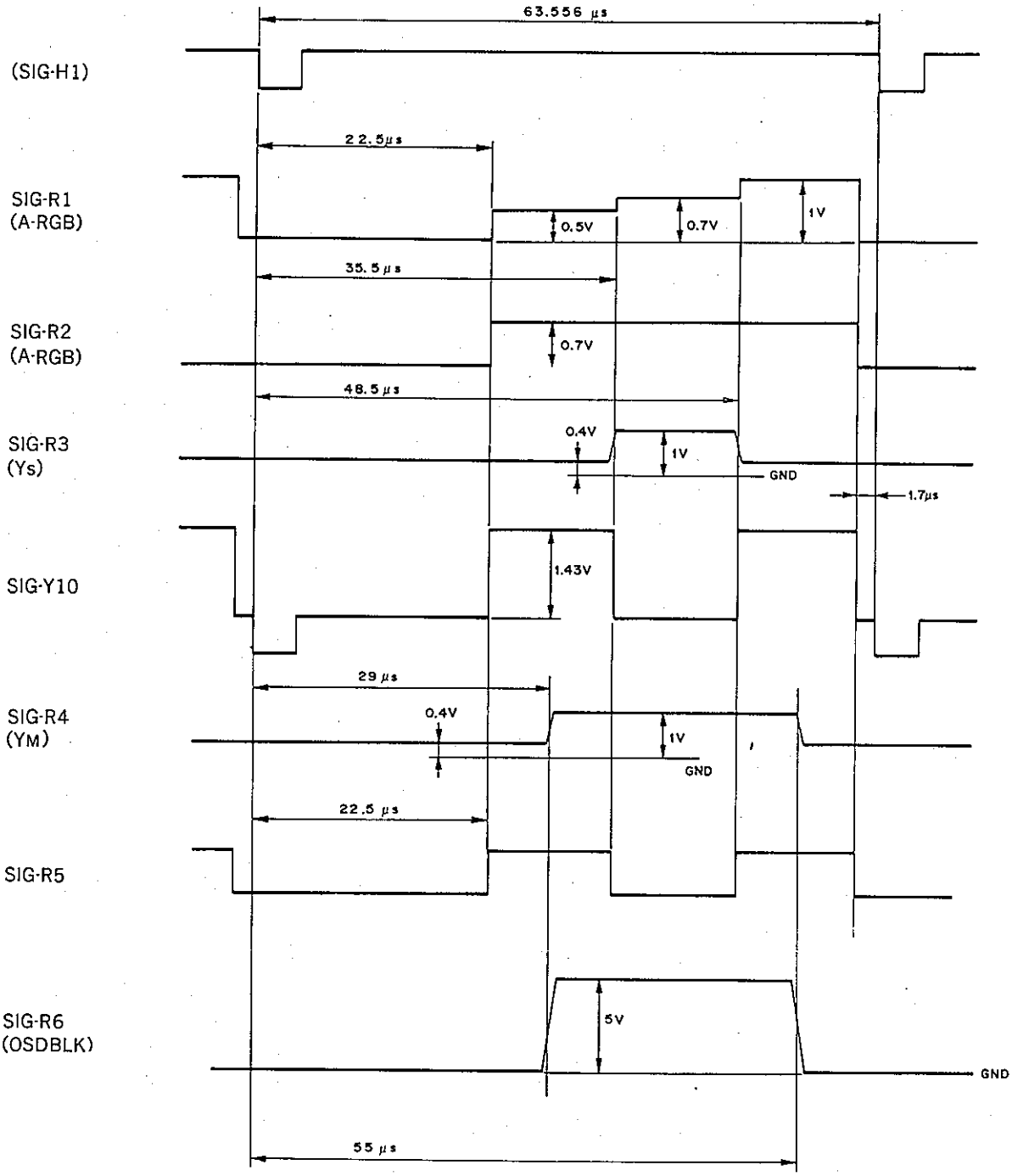
Y system test signals

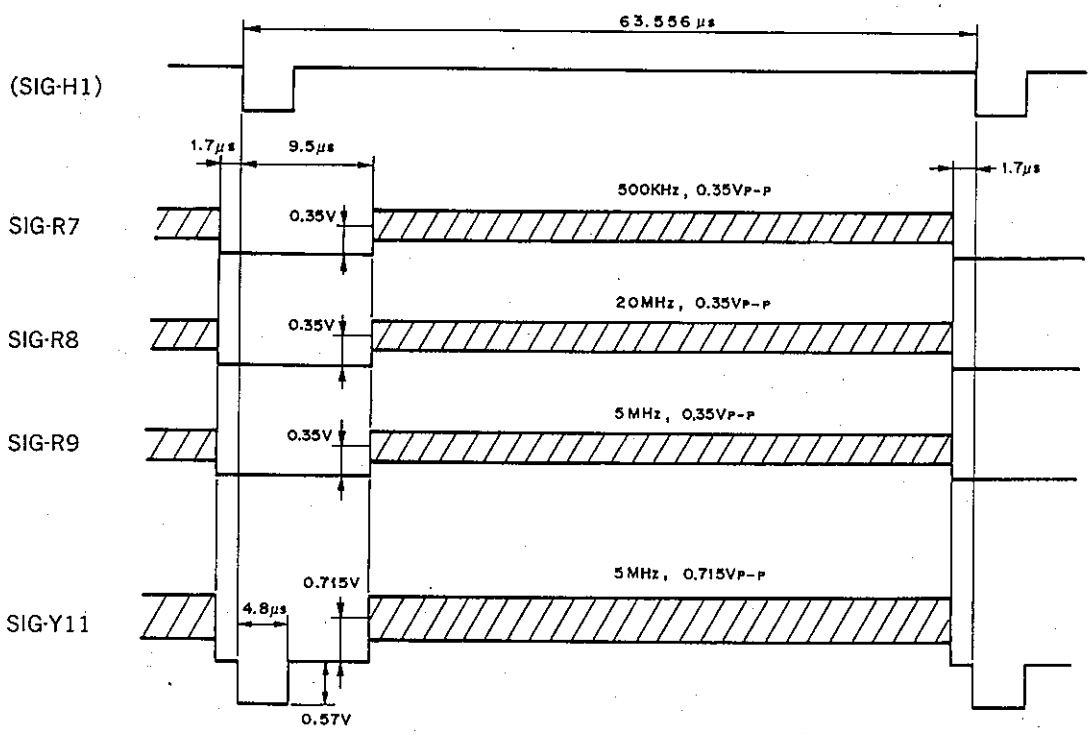


C system test signals f_{SC}=3.579545MHz



RGB system test signals




63.556 µs
(SIG-H1)
1.7µs
9.5µs
1.7µs
500KHz, 0.35VP-P
SIG-R7
0.35V
20MHz, 0.35VP-P
SIG-R8
0.35V
5MHz, 0.35VP-P
SIG-R9
0.35V
5MHz, 0.715VP-P
0.715V
SIG-Y11
4.8µs
0.57V

Test Methods

I²C Bus Register Data Initial Settings

Register Name	No. of Bit	Initial Setting	Description	Register Name	No. of Bit	Initial Setting	Description
HFREQ	7	Adjustment point		BAMP	5	$1F_H$	Maximum value
PMUTE	1	1_H	Canceling picture muting	GCUTOFF	4	F_H	Maximum value
VFREQ	5	Adjustment point		OFFNR	1	1_H	R output ON
VSMO	1	1_H	V pull-in 55 to 65Hz	OFFNG	1	1_H	G output ON
VTRIG	1	0_H	V trigger Pin 44	OFFNB	1	1_H	B output ON
VSHIFT	5	F_H	Center point	BCUTOFF	4	F_H	Maximum value
OFFNV	1	1_H	Delivering VD output	DYCOL	1	0_H	New dynamic color OFF
VSIZE	6	$1F_H$	Center point	RGB	2	0_H	Normal mode
VLIN	4	7_H	Center point	CHRTRAP	6	Adjustment point	
VCOMP	3	3_H	Center point	OFFCT	1	1_H	Chroma trap OFF
HPHASE	4	7_H	Center point	PICTURE	7	$7F_H$	Maximum value
AFC	2	0_H	Loop gain in effect	HUE	7	Adjustment point	
HSIZE	5	F_H	Center point	SATURATION	7	$7F_H$	Maximum value
REF	0	2_H	Minimum value	OFFTOT	1	0_H	Passed through TOT filter
PINAMP	5	F_H	Center point	BRIGHTNESS	7	$3F_H$	Center point
CORNER PIN	3	3_H	Center point	BLM	1	1_H	Picture ABL mode
PIN PHASE	4	7_H	Center point	SHARPNESS	4	7_H	Center point
VS CORR	4	7_H	Center point	RGBPIX	7	$7F_H$	Maximum value
GAMP	5	IF_H	Maximum value	DRGBP	1	0_H	0dB
ALIGN	1	0_H	Ordinary mode	CTL	8	0_H	Minimum value

Adjustment Method

1. HFREQ
   Set the same condition as for Electrical Characteristics No.5 Horizontal Oscillation Variable Range 1 and adjust HFREQ so that the frequency at Pin 37 will have data closest to 15.734kHz.

2. VFREQ
   Set the same condition as for Electrical Characteristics No.27 Vertical Oscillation Variable Range 1 and adjust VFREQ so that the frequency at Pin 29 will have data closest to 55Hz.

3. CHRTRAP
   Set the same condition as for Electrical Characteristics No.59 Chroma Trap Attenuation (OFFCT=0) and adjsut CHRTRAP so that U_{CTI} will be reduced to a minimum.

4. HUE
   Set the same condition as for Electrical Characteristics No.86 HUE Variable Range 1 (Video In: Sig-C4) and adjsut HUE so that V_{C2}-C_{C1} will be reduced to a minimum.

Operation

1. Synchronizing and deflection compensation systems

The video signals (2Vp-p standard) input to Pins 44 and 45 are led to the horizontal and vertical sync separator circuits for sync separation. First the horizontal sync signal obtained by the horizontal sync separator circuit is compared with the horizontal oscillation output to detect a phase difference. The error voltage resulting from the phase difference is minimized by the lag-lead filter which attenuates medium and high region components before application to the horizontal oscillator. The horizontal oscillator output is phase shifted to match the phase of the flyback transformer before it is output to Pin 37.

The vertical sync signal obtained by the vertical sync separator circuit is used to trigger the vertical oscillator for sychronization with the input signal. To ensure that the amplitude of the saw-tooth wave output of the vertical oscillator is maintained constant irrespective of the vertical frequency of the input, AGC is achieved before the output is delivered to the picture distortion correction circuit. The picture distortion correction circuit produces vertical saw-tooth wave and parabolic wave which are respectively output to Pins 31 and 32. Note that the horizontal and vertical oscillators require respective free running frequency adjustments.

The burst gate pulse produced by differentiation of the horizontal sync separated signal is supplied to the Y/C system block.

[Caution]

- When the Y/C and RGB interface systems are to be tested for evaluation, make sure that the free running frequencies of the horizontal and vertical oscillators are adjusted beforehand.

2. Y/C system

The Y signal (specified input level 2Vp-p) input to Pin 3 is passed through the delay line, sharpness control, clamp, dynamic picture and contrast control circuits and is mixed with color difference signal and is passed through the clamp circuit again before it is input to the RGB interface system block. The dynamic picture circuit pulls 50 IRE or lower signals toward the black side so that the black peak hold signal at Pin 8 will be at the pedestal level. Since a built-in chroma trap is provided, video signal can be directly input. The trap frequency shoud be adjusted by the I^2C bus register. In this case, the delay amount of the delay line and the peaking frequency of the sharpness control are simultaneously adjusted.

The chroma signal (specified input level, burst 500mVp-p, or video signal 2Vp-p) input from Pin 5 is passed through the TOT, ACC, color control (saturation control), killer circuit, etc.,and the burst locked VCO oscillation output is detected as the carrier. The signal is then fed to the matrix circuit for separation of color difference signals R-Y, B-Y and G-Y and fed through the Y/C mix circuit to provide R, G and B outputs.

[Caution]

- The chroma trap can be switched between the ON and OFF states. Even when it is to be used in the OFF state, it should first be placed in the ON state and the trap point adjusted to 3.58Hz for adjustment of the delay line, sharpness control, etc.
- The TOT (chroma BPF) can be switched between the ON and OFF states but it should be normally used in the ON state.
- Picture control is achieved for Y signal contrast control and chroma signal color control.

3. RGB interface system

Analog R, G and B signals input from Pins 16, 17 and 18 are led through the contrast control and clamp circuits and switched to the R, G and B signals of the Y/C system block. Thereafter, the R, G and B signals from Pins 10, 11 and 12 are added. The signals are then passed through the new dynamic color, brightness control, white balance drive amplifier, auto cut-off DC level shift and blanking control circuits to output R, G and B primary color signals from Pins 20, 22 and 24. The new dynamic color circuit detects the flesh and white colors from the amplitude ratio of R, G and B primary color signals and changes the ratio of the R, G and B outputs so that the color temperature will be higher as the color is closer to white without changing the color temperature of the flesh colored portion. (The circuit can be switched between the ON and OFF states by the I²C bus register.) The digital R, G and B signals are mainly used for screen display of channels, etc.

Switchover between the analog R, G and B signals and the R, G and B signals of the Y/C block is made by the I²C bus register and signal input to the Ys pin at Pin 15. The signal input to the Y_M pin at Pin 14, is used for half blanking of the R, G and B signals of the Y/C block (approx. −6dB). As for thre Y_S/Y_M for the digital R, G and B signals, the signal input to the OSDBLK Pin at Pin 9, is used. The attenuation of the R, G and B signals depends on the voltage to be input.

The signal input to Pin 26 is compared with the internal reference voltage and is then integrated by the capacitor connected to Pin 27 for control of picture and brightness. Switchover between the picture ABL mode and the combined picture ABL and brightness ABL mode can be made by the I²C bus register.

[Caution]

- When the digital R, G and B signals and OSDBLK signal are not to be used, connect Pins 9, 10, 11 and 12 to GND.

[About auto cut-off]

For white balance, drive control (R, G and B output gain control) and cut-off control (black side DC level control) are involved. The CXA1312S or CXA1313S uses the I²C bus register for drive control. For cut-off control, a loop is formed between the IC and CRT to achieve auto cut-off control. The auto cut-off arrangement makes it possible to compensate for the change of the CRT with time. To absorb the variability of the CRT, the G and B outputs are led to the I²C bus register for adjustment of the cut-off voltage.

The auto cut-off loop is configured as described below.

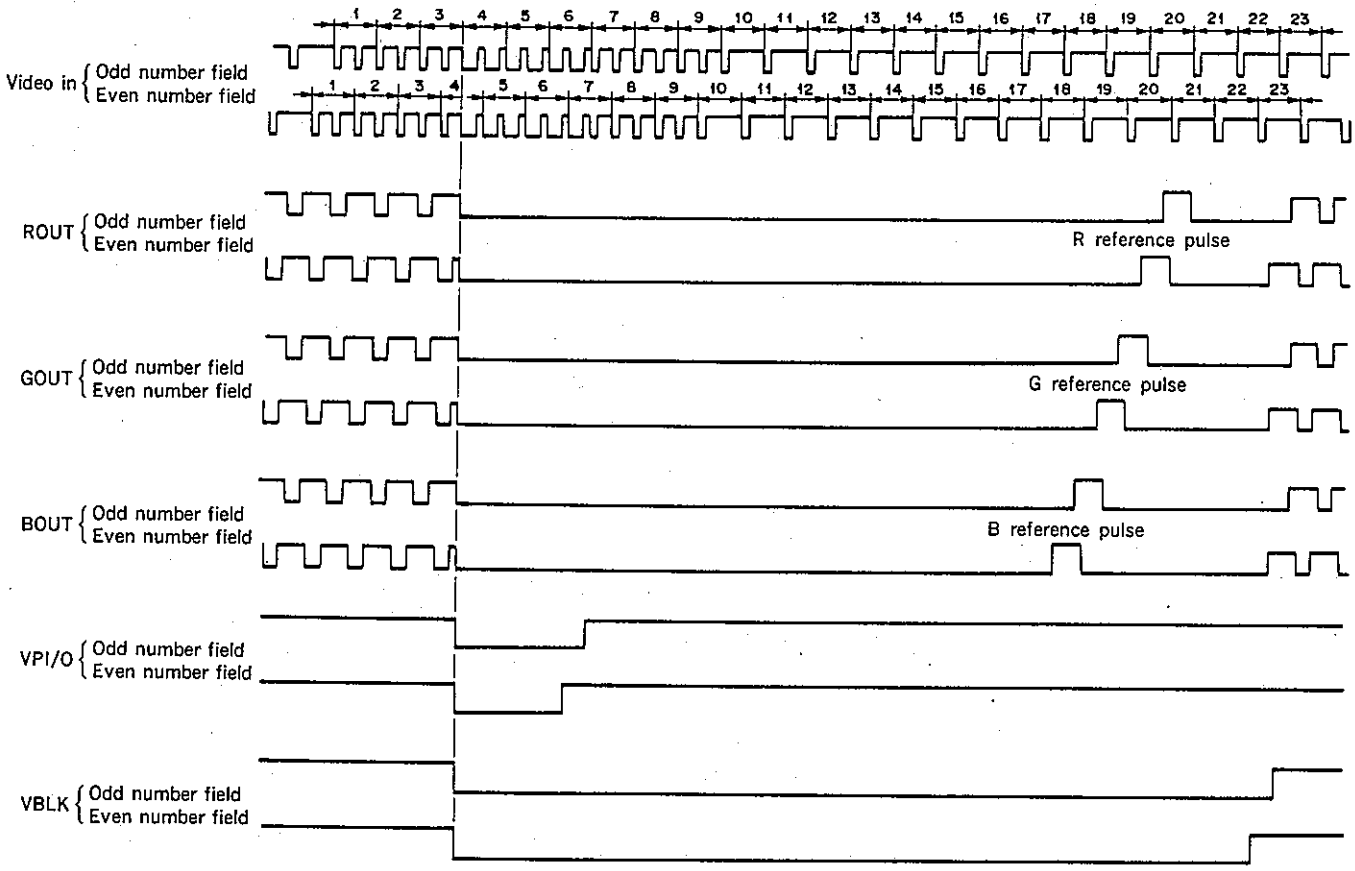
- The B, G and R reference pulses for auto cut-off, shifted 1H each in the order mentioned, are added to the top of picture.
- The 1k of each of the R, G and B outputs is converted into a voltage before it is input to Pin 25.
- The voltage input to Pin 25 is compared with the reference voltage in the IC to change the DC level of reference pulse.
  (The DC level is changed by changing the DC shift amout of each of the R, G and B outputs.)

The loop mentioned above determines the DC shift amout of each of the R, G and B outputs and lets the capacities connected to Pins 19, 21 and 23 hold the DC shift amounts during the 1V section. If the voltage at any of the Pins 19, 21 and 23 is less than 4.2V, the R, G and B outputs except the referencee pulses are blanked. The positions of reference pulses can be changed by the I²C bus register.

Positions of reference pulses

REF	Pin 40: 0V			Pin 40: 4.5V			Pin 40: 9V		
	R	G	B	R	G	B	R	G	B
00	20H	19H	18H	27H	26H	25H	34H	33H	32H
01	22H	21H	20H	30H	29H	28H	38H	37H	36H
10	24H	23H	22H	33H	32H	31H	42H	41H	40H
11	26H	25H	24H	36H	35H	34H	46H	45H	44H

R, G and B output V blanking and VBLK go low at 3H and go high (V blanking canceled) at R reference pulse position +3H.



Automatic cut-off reference pulse time chart (Ref; Pins 0 and 40: 0V)

[Picture muting mode]

- Mode where all, including reference pulses, are picture muted
  - When XRAY is input
  - PMUTE: 0
  - OFFNV: 0
- Mode where all except reference pulses are picture muted
  - OFFNR: 0 (ROUT only)
  - OFFNG: 0 (GOUT only)
  - OFFNB: 0 (BOUT only)
  - When Ik pin voltage is so low that S/H pin voltage at any of Pins 19, 21 and 23 is lower than 4.2V

Definition of I²C Bus Register

Slave addreses

88_H: SLAVE RECEIVER
89_H: SLAVE TRANSMITTER

Register table

- All registers are set at 0 when the IC is reset.
- '*' is not defined.

[Control registers]

Sub Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
XXX00000	HFREQ							PMUTE
XXX00001	VFREQ					*	VSMO	VTRIG
XXX00010	VSHIFT					*	*	OFFNV
XXX00011	VSIZE						*	*
XXX00100	VLIN				*	VCOMP		
XXX00101	HPHASE				*	*	AFC	
XXX00110	HSIZE					*	REF	
XXX00111	PINAMP					CORNER PIN		
XXX01000	PIN PHASE				VS CORR			
XXX01001	GAMP					*	0	ALIGN
XXX01010	BAMP					*	*	*
XXX01011	GCUTOFF				*	OFFNR	OFFNG	OFFNB
XXX01100	BCUTOFF				*	DYCOL	RGB	
XXX01101	CHRTRAP						*	OFFCT
XXX01110	PICTURE							*
XXX01111	HUE							*
XXX10000	SATURATION							OFFTOT
XXX10001	BRIGHTNESS							BLM
XXX10010	SHARPNESS				*	*	*	*
XXX10011	RGBPIX							DRGBP
XXX11100	CTL							

[Status register]

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1st byte	PONRES	HLOCKN	HCENT	0	0	IK	0	0
2st byte	RET							

Description of Registers

H FREQ (7): H f_o adjustment
0=Maximum frequency
127=Minimum frequency

P MUTE (1): Picture muting ON/OFF
0=Picture muting ON (Auto cut-off reference pulse is also muted.)
1=Picture muting OFF

V FREQ (5): V f_o adjustment
0=Maximum frequency
31=Minimum frequency

VSMO (1): To switch between V lock ranges
0=Normal range (Pull-in range=55 to 65Hz)
1=Wide range (Pull-in range=45 to 75Hz)

VTRIG (1): To switch internal and external V triggers and input and output definitions
0=To derive V trigger from inside (Pin 29 to serve as output)
1=To input V trigger from outside (Pin 29) (Pin 29 to serve as input)

V SHIFT (5): V shift
0=To raise
31=To lower

OFFNV (1): V-OUT ON/OFF
0=Stops outputting V-OUT (At the same time, picture muting begins. In the picture muting mode, the reference pulse for auto cut-off is also muted.)
1=Outputs V-OUT

V SIZE (6): V size
0=Minimum
63=Maximum

V LINEARITY (4): V linearity
0=To compress upper part of picture and expand lower part of picture
15=To expand upper part of picture and compress lower part of picture

V COMP (3): V zooming correction
0=Minimum
7=Maximum

H PHASE (4): H center
0=To move picture to maximum left-sided position
15=To move picture to maximum right-sided position

AFC (2): To switch AFC

AFC1	AFC0	
0	0	AFC loop gain intermediate
0	1	AFC loop gain small
1	0	AFC loop gain large
1	1	AFC loop open

H-SIZE (5): H size
0=Minimum
31=Maximum

REF (2): To switch auto cut-off reference pulse position

REF1	REF0	
0	0	B=18H, G=19H, R=20H
0	1	B=20H, G=21H, R=22H
1	0	B=22H, G=23H, R=24H
1	1	B=24H, G=25H, R=26H

PIN AMP (5): Pin amp.
0=Minimum
31=Maximum

CORNER PIN (3): Corner pin
0=Minimum
31=Maximum

PIN PHASE (4): Pin phase
0=To widen upper part of picture and narrow lower part of picture
15=To narrow upper part of picture and widen lower part of picture

VS CORR (4): S-correction of V
0=Minimum
31=Maximum

G AMP (5): To adjust green drive (red drive fixed)
0=Minimum gain
31=Maximum gain

ALIGN (1): To switch between HCENT status register valid and invalid
0=HCENT invalid (Normal mode)
1=HCENT valid (H-FREQ adjustment mode)

B AMP (5): To adjust blue drive (red drive fixed)
0=Minimum gain
31=Maximum gain

G CUT OFF (4): To adjust green cut-off voltage (red cut-off voltage fixed)
0=Minimum
15=Maximum

OFFNR (1): Red output ON/OFF
0=Red output OFF
1=Red output ON

OFFNG (1): Green output ON/OFF
0=Green output OFF
1=Green output ON

OFFNB (1): Blue output ON/OFF
0=Blue output OFF
1=Blue output ON

B CUTOFF (4): To adjust blue cutoff voltage (read cut off voltage fixed)
0=Minimum
15=Maximum

DYCOL (1): New dynamic color (12500K) ON/OFF
0=New dynamic color OFF
1=New dynamic color ON

RGB (2): To switch RGB source

RGB1	RGB0	
0	0	To select TV or external R, G and B inputs (Pins 16 through 18). There are switched by Y_S (Pin 15).
1	0	To select external R, G and B inputs
—	1	To select TV

CHRTRAP (6): To adjust Y/C system filters such as 3.58MHz chroma trap
0=Minimum trap frequency
63=Maximum trap frequency

OFFCT (1): Chroma trap ON/OFF
0=Chroma trap ON
1=Chroma trap OFF

PICTURE (7): Picture
0=Minimum
127=Maximum

HUE (7): Hue
0=Flesh color nearer to green
127=Flesh color nearer to red

SATURATION (7): Color
0=Minimum
127=Maximum

OFFTOT (1): TOT filter ON/OFF
0=To pass through TOT filter
1=To bypass TOT filter

BRIGHTNESS (7): Brightness
0=Minimum
127=Maximum

BLM (1): To switch ABL mode
0=Combined picture ABL and brightness ABL mode
1=Picture ABL (including brightness ABL for protection)

SHARPNESS (4): Sharpness
0=Minimum sharpness gain
15=Maximum sharpness gain

RGB PICTURE (7): Picture of external R, G and B inputs (Pins 16 through 18)
0=Minimum
127=Maximum

DRGBP (1): To switch brightness of external digital R, G and B inputs for screen display
0=0dB
1=−3dB

CTL (8): Used for testing I²C bus decoder

PONRES (1): To detect POWER ON RESET
0=Set at 0 after master has read this status via bus
1=Set at 1 when power is turned on or when power dip occurs

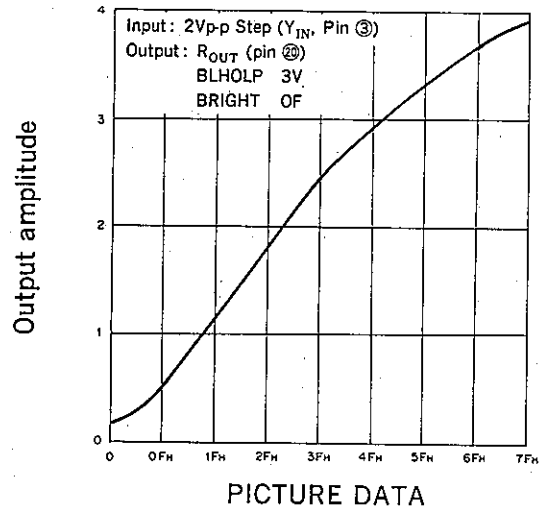
HLOCKN (1): To return H f_O status to indicate whether it is locked or not locked to H frequency of signal during H f_O adjustment
0=Not locked to H of signal
1=Locked to H of signal

HCENT (1): To return H f_O relation to indicate whether it is smaller or large than H frequency of signal during H f_O adjustment
0=$F_{OSC} < F_H$ (signal input)
1=$F_{OSC} > F_H$ (signal input)

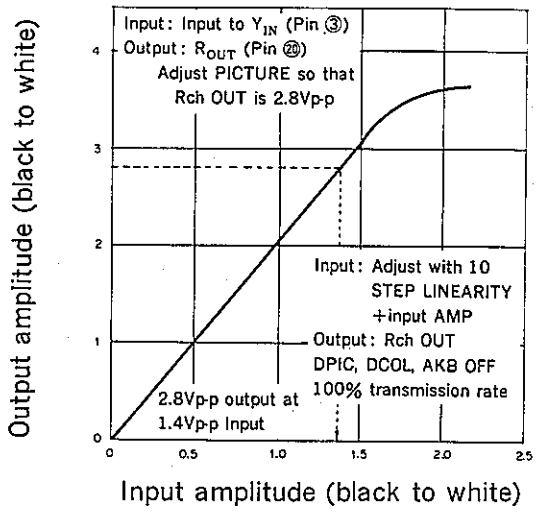
IK (1): To return Ik current status to indicate whether it is stable or not
0=All Ik currents of R, G and B in stable state
1=Ik currents unstable

RET (8): Used for testing I²C bus decoder. Data written into the CTL register is directly returned.

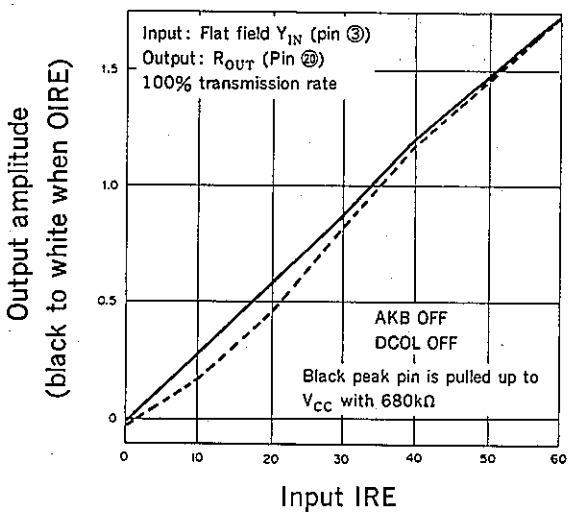
Picture control characteristics



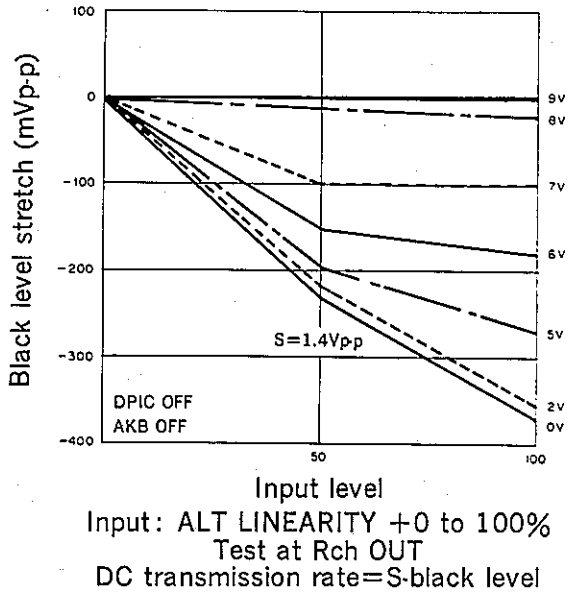
I/O characteristics



I/O characteristics of auto pedestal close loop

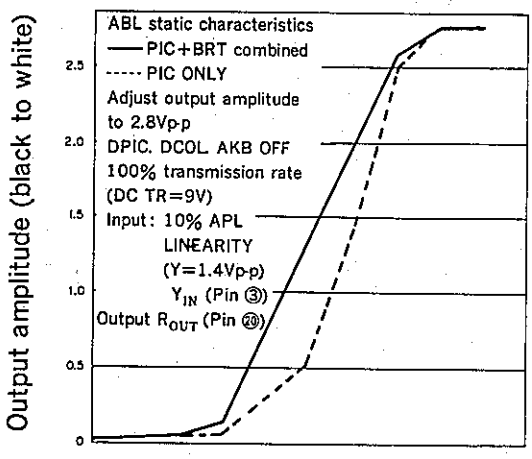


DC transmission ratio

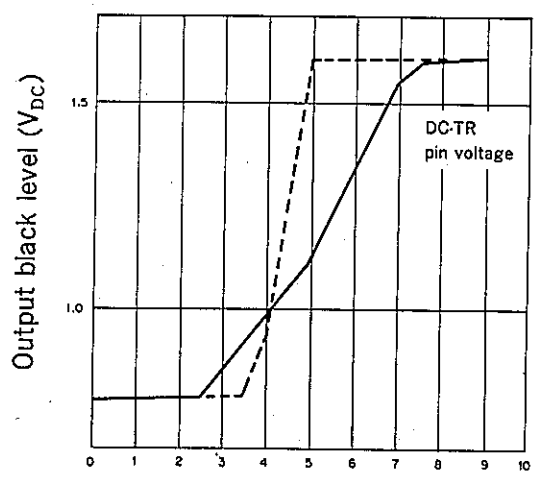


Input: ALT LINEARITY +0 to 100%
Test at Rch OUT
DC transmission rate=S-black level

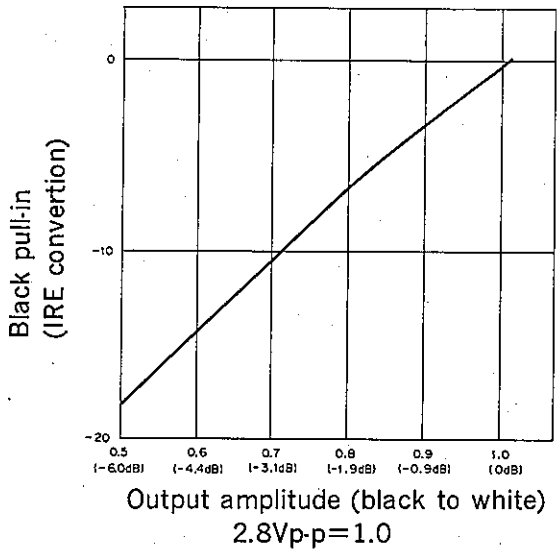
ABL static characteristics (amplitude)



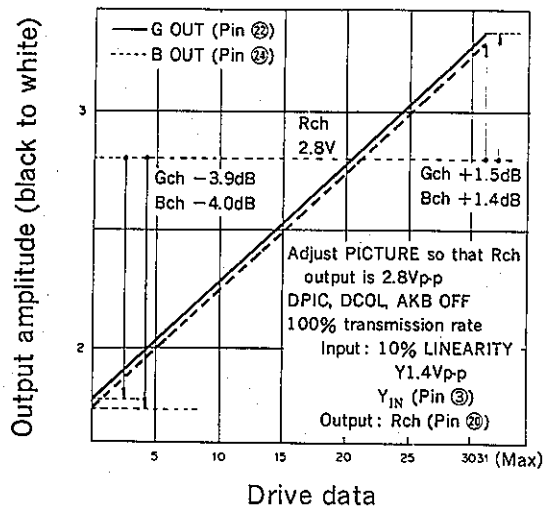
ABL static characteristics (black level)



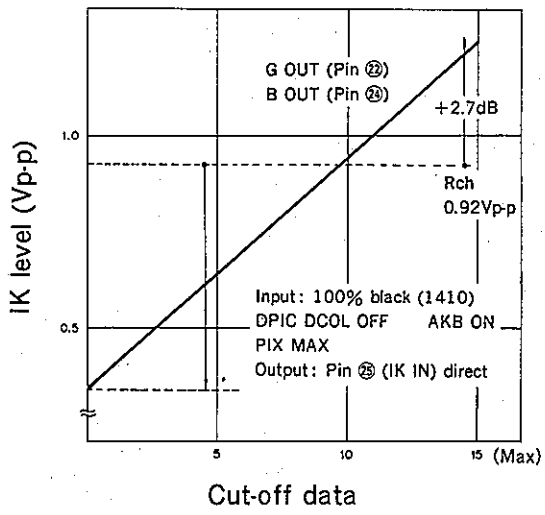
Pull-in at PIC+BRT ABL combined mode

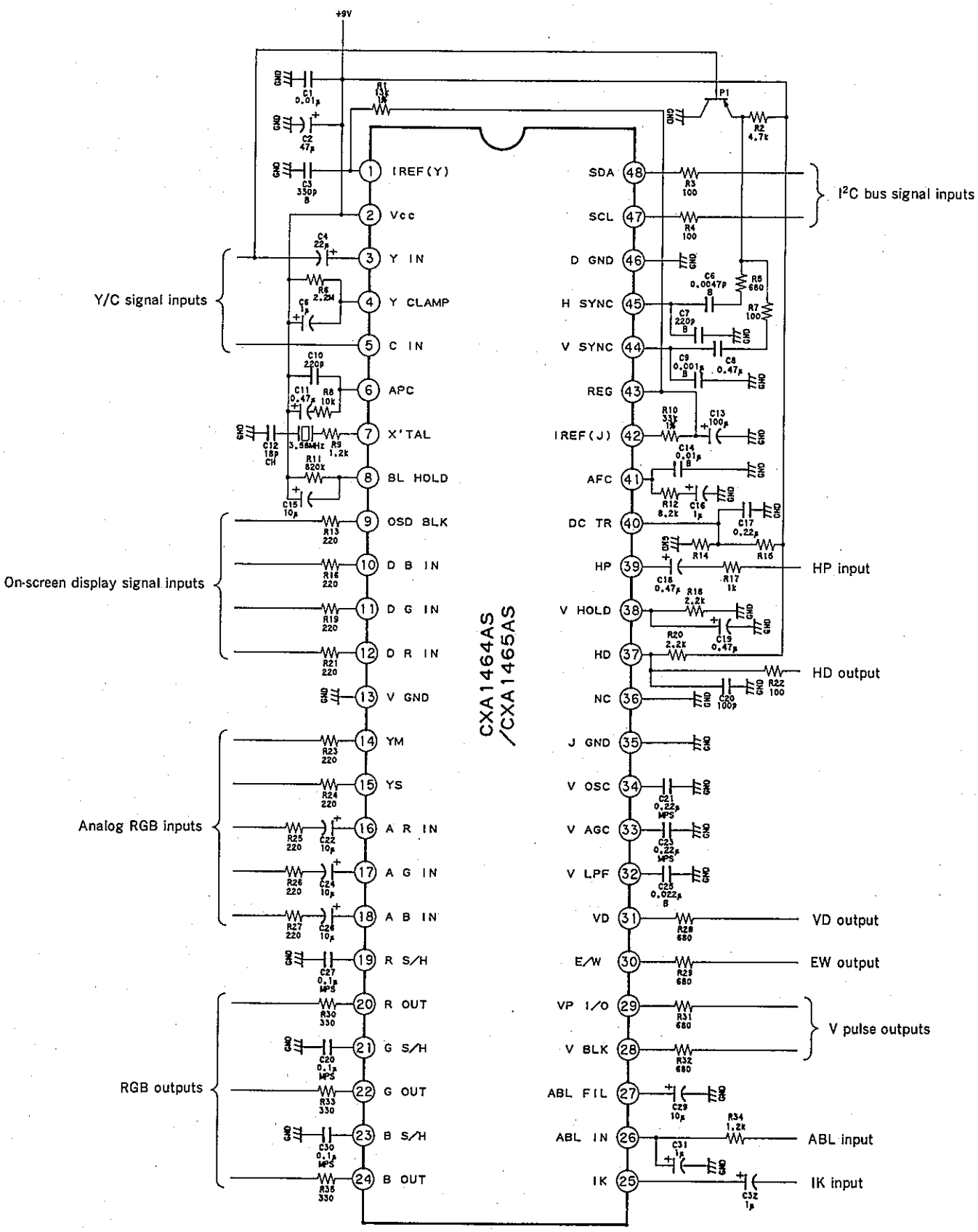


Drive control characteristics



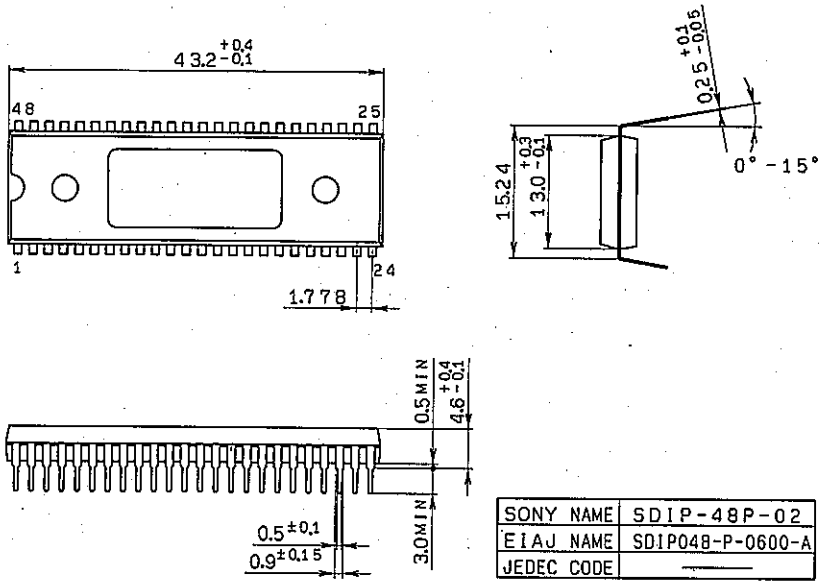
Cut-off control characteristics




CXA1464AS
/CXA1465AS
1 IREF(Y)
2 Vcc
3 Y IN
4 Y CLAMP
5 C IN
6 APC
7 X'TAL
8 BL HOLD
9 OSD BLK
10 D B IN
11 D G IN
12 D R IN
13 V GND
14 YM
15 YS
16 A R IN
17 A G IN
18 A B IN
19 R S/H
20 R OUT
21 G S/H
22 G OUT
23 B S/H
24 B OUT
25 IK
26 ABL IN
27 ABL FIL
28 V BLK
29 VP I/O
30 E/W
31 VD
32 V LPF
33 V AGC
34 V OSC
35 J GND
36 NC
37 HD
38 V HOLD
39 HP
40 DC TR
41 AFC
42 IREF(J)
43 REG
44 V SYNC
45 H SYNC
46 D GND
47 SCL
48 SDA
Y/C signal inputs
On-screen display signal inputs
Analog RGB inputs
RGB outputs
I²C bus signal inputs
HP input
HD output
VD output
EW output
V pulse outputs
ABL input
IK input

Package Outline Unit: mm

48pin SDIP (Plastic) 600mil 5.1g



SONY NAME	SDIP-48P-02
EIAJ NAME	SDIP048-P-0600-A
JEDEC CODE	———

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).